Amorphous Zinc-Oxide-Based Thin-film Transistors
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Recently, RF-sputtered zinc oxide-based field effect transistors (FETs) have been demonstrated with higher mobilities and performance than amorphous silicon, the dominant material used for display backplanes [1,2]. The low temperature processing possible for zinc oxide-based FETs [3] makes these materials compatible with flexible polymer substrates, but patterning with shadow masks limits feature size and accuracy. This project aims to develop a low-temperature, lithographic process for zinc oxide-based FETs, similar to one developed for organic FETs [4].

Our initial work focuses on two issues: determining optimal conditions for (1) growing the oxide semiconductor and (2) depositing high-quality oxide semiconductor and contact films on an organic polymer, parylene. For the former, top-contact, bottom gate ZnO FETs were fabricated on Si/SiO\textsubscript{2} substrates, using SiO\textsubscript{2} as the gate dielectric, Si as the gate, and sputtered indium-tin-oxide (ITO) as source/drain contacts. The RF sputtering power, total chamber pressure, and annealing temperatures were varied in a series of experiments; Figure 1 shows the current-voltage characteristics of a device from one set of conditions.

To determine optimal conditions for depositing high-quality films on an organic polymer, ITO films were deposited on an organic polymer dielectric, parylene, at different sputter rates. High stress in the oxide films on top of the soft organic polymer dielectric, parylene, may cause cracking and discontinuities in the film. Figure 2a shows a microscope photograph of the cracked surface of an ITO film sputtered at 80W on parylene; Figure 2b shows a continuous ITO film sputtered at 15W on parylene.

REnERENCES