Machine vision requires an image sensor able to capture natural scenes which may have a dynamic range as high as four orders of magnitude. Reported wide dynamic range image sensors suffer from some or all of the following problems: large silicon area, high cost, low spatial resolution, small dynamic range increase factor, poor pixel sensitivity, small intensity resolution, etc. The primary focus of this research is to develop a single-chip imager for machine vision applications which addresses these problems, but is still able to provide an ultra wide intensity dynamic range by implementing a novel pixel-by-pixel automatic exposure control. The secondary focus of the research is to make the imager programmable, so that its performance (light intensity dynamic range, spatial resolution, light intensity resolution, frame rate, etc.) can be tailored to suit a particular machine vision application.

The image sensing array has pixels which can be independently read and reset. The proposed brightness adaptive algorithm then predictive and scales the voltage in photodiodes that would saturate under normal circumstances based on information gathered in several readout checks. The total integration time is subdivided into several integration times (called integration slots). These integration slots are progressively shorter, and if in any of the checks it is determined that the pixel will saturate at the end of the current integration slot, then the pixel is reset and it is allowed to once more integrate light, but for a shorter period of time. Each pixel has a small associated memory location outside of the pixel array needed to store an exponent which identifies the actual integration slot used. This information is used to appropriately scale the digitized pixel output.

A Programmable, Wide Dynamic Range CMOS Imager with On-Chip Automatic Exposure Control

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Passive pixel sensors provide an alternative to the conventional Active Pixel Sensor (APS) for high-density CMOS imaging arrays. Similar to the history of the single-transistor DRAM cell, this one-transistor pixel cell boasts one main advantage over the APS. It can achieve a high fill-factor in a smaller area, leading to a high-density array of pixels with high quantum efficiency. Experiments reveal a major weakness in passive pixels is a signal-dependent parasitic current that can contaminate charge signals in different parts of the array. In this project, we explain the origin of this parasitic current and demonstrate a Correlated Double Sampling (CDS) circuit in a differential architecture that removes its effects.

Figure 12 illustrates the passive pixel architecture and cross-section. The passive pixel consists of a high-efficiency n-well photodiode and one transistor for reset and row select. The charge difference between the output of a sensing pixel and a dummy cell kept in the dark is converted to a voltage with a sense amplifier at the bottom of every column. This differential architecture is advantageous in rejecting any common-mode signals such as ground bounce.

Passive pixels are plagued with a signal-dependent parasitic current caused by photogenerated electrons collected by the reverse-biased junction of the column line at each pixel. The combined effect of the charge leakage from 256 cells on the column line can be significant and will appear as a parasitic current at each column line. This parasitic current, which is also present in active pixel arrays, is catastrophic in passive pixels because charge-to-voltage conversion does not occur within the pixel. The parasitic charge of a bright pixel can thus contaminate the output of a dark pixel in other rows in the column line and cause smear in the image.

Two strategies were used to remove the effects of the parasitic current. The first was at the architectural level where a differential readout between a sensing and a
dummy column rejects the parasitic current that is common between the two columns. The second part consisted of removing the difference in parasitic currents between adjacent columns. The latter was achieved with a CDS circuit that senses the signal with the parasitic current during the first sample phase and then senses the parasitic current only during the second sample phase. The difference between the output of these two sample phases then purely corresponds to the pixel signal and is no longer dependent on the parasitic current.

The improvements achieved with the differential CDS circuit were quantified in terms of column-to-column Fixed-Pattern Noise (FPN). As expected, the dark FPN values are similar at 0.4% with and without CDS. The difference becomes more pronounced as the light intensity increases and the parasitic current mismatches result in a much higher FPN in the absence of the differential CDS circuit.

Fig.12: A CMOS passive pixel imager. (a) Architecture. (b) Pixel cross-section.