Analog circuits and digital circuits have, for the most of history, been fabricated on separate substrates in electronic systems. However, the drive for higher performance, lower cost, and lower power have pushed for the integration of these two parts onto a single microchip. While plausible and feasible, the marriage of the two is not without problems and difficulties. One of the most insidious problems is the substrate noise coupling from the highly noise tolerant digital circuits to the extremely noise sensitive analog circuits. Digital noise can severely degrade crucial analog performance if not contained properly.

Up to now, most efforts of minimizing digital noise effects on analog circuitry have been to utilize good layout techniques and fully-differential analog signal paths along with computer-aided-design verification. Although this process ensures the mixed-signal system performs as desired, no real effort has been made to design circuits that pointedly address the substrate noise problem.

Therefore, the focus of this research is to characterize and investigate digital noise mitigating circuit techniques, in the digital and analog domains. The benefit of easily integrating analog and digital circuits would be immense and epochal.

In our approach, we propose to shape the digital noise out of the band of sensitive analog circuits. This is possible by monitoring and manipulating digital transitions or capacitively coupling anti-noise signal to the substrate in order to cancel noise in the band of interest. We are exploring both possibilities using a digital noise shaping technique similar to delta-sigma modulation.

Superconducting Bandpass Delta-Sigma A/D Converter

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The direct digitization of RF signals in the GHz range is a challenging application for any circuit technology. Traditionally, flash A/D converters have been used to digitize signal frequencies above 1 GHz, but their resolution and linearity are inadequate for most radio systems, which must handle signals with a large dynamic range. Semiconductor bandpass delta-sigma converters are used to digitize IF signals with high resolution, but their performance at microwave frequencies is limited by the speed of semiconductor comparators and the low Q of integrated inductors.

In this program, we present the design of a superconducting bandpass delta-sigma converter for direct A/D conversion of GHz RF signals. The schematic of the circuit is shown in Figure 15. The input signal is capacitively coupled to one end of a superconducting microstrip transmission line, which serves as a high quality resonator (loaded Q > 5000). The current flowing out of the other end of the microstrip line is quantized by a clocked comparator comprising two Josephson junctions. If the current is above threshold, the lower junction switches and produces a quantized voltage pulse known as a Single Flux Quantum (SFQ) pulse. If the current is below threshold, the upper junction switches instead. The pattern of voltage pulses generated across the lower Josephson junction represents the digital output code of the delta-sigma modulator. These voltage pulses also inject current back into the microstrip line, providing the necessary “feedback” signal to the resonator. At the quarter-wave resonance of the microstrip line (about 2 GHz in our design), the resonator shunts the lower junction with a very low impedance, the “feedback” current to the resonator is maximized, and the quantization noise is minimized. Because of the high speed of Josephson junctions and the simplicity of the proposed circuit, we expect sampling frequencies in excess of 20 GHz, limited only by the digital circuitry needed to process the output of the delta-sigma modulator.
Circuit performance at a 20 GHz sampling rate has been evaluated with JSIM, a SPICE-like simulator for superconducting circuits. A representative example of the A/D converter’s output spectrum is shown in Figure 16. In this simulation, the A/D converter was driven by a large (-0.8 dBFS) input near 2.13 GHz, just above the frequency band of interest. The minimum in the quantization noise power spectrum is located at 2.05 GHz. Inband noise is -53 dBFS and -57 dBFS over bandwidths of 39 MHz and 19.5 MHz, respectively. In addition to the minimum at 2.05 GHz, there are minima at other frequencies. Near dc, bias inductor Lbias shunts the lower Josephson junction of the comparator with a low impedance, and quantization noise is minimized. The other minima correspond to higher-order modes on the microstrip line, including some above 10 GHz which appear in the digital domain as “aliased” modes. In principle, these aliased modes could interfere with the desired noise shaping near 2 GHz. In our design, the sampling frequency and the resonances of the microstrip line have been chosen so that no aliased modes fall near the band of interest. InterModulation (IM) distortion was also studied with several long JSIM simulations. Over a 39 MHz bandwidth, in-band IM distortion is better than -69 dBFS. Other features of the circuit include unconditional stability and a full-scale input sensitivity of 20 mV (rms).

While a 20 GHz sampling rate improves the performance of delta-sigma converters, the challenges of high speed testing in a cryogenic environment are formidable. Even in the best cryogenic sample holders, the long cables used to connect the superconducting chip to room-temperature electronics have significant losses at frequencies above 10 GHz. In previous reports, we described an optoelectronic clocking technique, which bypasses the bandwidth limitations of conventional
electrical testing. In this approach, picosecond optical pulses from a mode-locked laser are delivered (via optical fiber) to an on-chip photodetector, which generates the clock pulses needed by the Josephson circuitry. We have already demonstrated our optoelectronic clocking system up to 20 GHz and will use it in testing our A/D converter later this year.

While the high speed clocking will be done optoelectronically, the digital outputs of the A/D converter will still be read out over standard coaxial cables. Consequently, direct transfer of the output of the delta-sigma modulator (at 20 Gbits/s) to the room-temperature test equipment is impractical in our setup. Instead, on-chip processing of the data will be used to reduce the bandwidth requirements for readout.

Two segments of the modulator’s bit stream will be captured with a pair of 128-bit shift registers. The number of clock cycles skipped between acquiring the two segments will be set by an on-chip programmable counter (from 0 to over 8000). Cross-correlation of the two captured segments will be used to provide estimates of the autocorrelation function R[n] of the A/D converter’s output, for all values of n up to 8000. Fourier transformation of R[n] will then yield a power spectrum with frequency resolution comparable to an 8K FFT of the original bit stream.

We have just recently completed the design and layout of our entire A/D converter test chip, including the band-pass delta-sigma modulator, the shift registers, the programmable counter, and readout circuitry. The chip has been fabricated at HYPRES, Inc., and we are in the process of evaluating the A/D converter and associated test circuits.