electrical testing. In this approach, picosecond optical pulses from a mode-locked laser are delivered (via optical fiber) to an on-chip photodetector, which generates the clock pulses needed by the Josephson circuitry. We have already demonstrated our optoelectronic clocking system up to 20 GHz and will use it in testing our A/D converter later this year.

While the high speed clocking will be done optoelectronically, the digital outputs of the A/D converter will still be read out over standard coaxial cables. Consequently, direct transfer of the output of the delta-sigma modulator (at 20 Gbits/s) to the room-temperature test equipment is impractical in our setup. Instead, on-chip processing of the data will be used to reduce the bandwidth requirements for readout.

Two segments of the modulator’s bit stream will be captured with a pair of 128-bit shift registers. The number of clock cycles skipped between acquiring the two segments will be set by an on-chip programmable counter (from 0 to over 8000). Cross-correlation of the two captured segments will be used to provide estimates of the autocorrelation function \( R[n] \) of the A/D converter’s output, for all values of \( n \) up to 8000. Fourier transformation of \( R[n] \) will then yield a power spectrum with frequency resolution comparable to an 8K FFT of the original bit stream.

We have just recently completed the design and layout of our entire A/D converter test chip, including the band-pass delta-sigma modulator, the shift registers, the programmable counter, and readout circuitry. The chip has been fabricated at HYPRES, Inc., and we are in the process of evaluating the A/D converter and associated test circuits.

Portable systems that depend on batteries have a limited operating life and are prone to failure at inconvenient times. We propose a system that uses ambient energy as a power source for an ultra low-power DSP that processes sensor data. The sensor algorithm is power scalable to trade off performance for system power. An example of power scalable processing is a low power DSP (Figure 17) for physiological monitoring. The biomedical sensor is a microphone for recording heartbeats, breathing sounds, and voice data. This data will eventually be used to determine the physical condition of the wearer. The first step is detection of the heartbeats, which can be used to determine heart rate as the basis for a physiological assessment.

Fig. 17: Die photograph of an ultra low-power DSP.
Evaluation of the spectrogram of the acoustic data indicates that most of the energy from heartbeat sounds lies in the low frequency range, below 200 Hz. We developed a classifier based approach to heartbeat detection that takes advantage of this spectral characteristic to improve detection performance in the presence of speech and other high frequency energy.

A complete system is being developed to demonstrate accurate detection of heartbeats at the predicted low power requirements. The system will include an analog sensor interface, a test data input, and a user interface that will allow for programming other biomedical sensing applications.

Clock skew and jitter continue to increase with scaling, and will consume an ever-larger fraction of the cycle time. We have developed a distributed clocking approach that allows faster clock speeds with lower random skew and jitter than possible with traditional clock tree distribution methods.

In our distributed clock approach, the clock signal is generated with phase locked loops at multiple points across a chip, and distribution happens only to small local tiles. Phase comparators at the boundaries of each tile produce an error signal that is summed by an amplifier in center of each tile and used to adjust the frequency of the node oscillator. Skew is introduced only by asymmetries in phase detectors instead of mismatches in physically separated buffers as with conventional tree based distribution. Also importantly, the clock is regenerated at each node, so jitter does not accumulate. To make this system functional, several issues had to be addressed including stability, power supply noise rejection, and locking. A proof of concept test chip (Figure 18) with 16 oscillators (4x4 array) was fabricated using 0.35 µm and showed stable operation at 1.4 GHz.

Active GHz Clock Network Using Distributed PLLs

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Fig. 18: Distributed clock test chip with 16 oscillators.