Drain Resistance Degradation in InAlAs/InGaAs Metamorphic HEMTs

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InAlAs/InGaAs High Electron Mobility Transistors (HEMT) hold promise for power-millimeter wave applications. A major reliability concern in some of these devices is the degradation of the drain resistance that is observed when the device is electrically stressed for a long time at bias conditions necessary for power applications. The goal of this project is to find the physical origin of this reliability problem and to suggest solutions to it.

State-of-the-art InAlAs/InGaAs metamorphic HEMTs (mHEMTs), provided by our sponsor, Hewlett Packard, were stressed under different bias schemes. It was found that several figures of merit of the device degrade under severe bias stress. In particular, the drain resistance, $R_D$, has been found to increase significantly. Experiments on mHEMTs have shown that the degradation of $R_D$ is strongly correlated to the amount of impact-ionization during stress.

![Figure 15: Time evolution of the drain resistance $R_D$ and the intrinsic transconductance $g_m$ of a HEMT during a step-stress experiment. The HEMT is stressed at a bias of $V_{DG0}$ that is stepped up from 1.7 to 4.6 V in 0.1 V intervals.](image)

Fig. 15: Time evolution of the drain resistance $R_D$ and the intrinsic transconductance $g_m$ of a HEMT during a step-stress experiment. The HEMT is stressed at a bias of $V_{DG0}$ that is stepped up from 1.7 to 4.6 V in 0.1 V intervals.
By studying mHEMTs with different layer-compositions, we have found that these devices show two different degradation modes. This is illustrated in the figure which shows the degradation of the drain resistance, $R_D$, and the intrinsic transconductance, $g_{mo}$, of a HEMT under step-stress, where the drain to gate voltage $V_{DG_{o}}$ has been stepped up from 1.7 V to 4.6 V. It can be seen that there is a first degradation mechanism, which starts at $V_{DG_{o}} \approx 1.8$ V and that causes both $g_{mo}$ and $R_D$ to degrade. A second degradation mechanism starts at $V_{DG_{o}} \approx 3.8$ V and causes only degradation of $R_D$.

We have carried out extensive experiments of this kind. They have allowed us to postulate that in the first degradation mechanism, hot electrons are trapped by defects at the etch-stopper or the barrier layer, depleting the sheet carrier concentration in the drain-side of the device. This causes degradation of $R_D$ and $g_{mo}$. In the second mechanism, hot electrons degrade the non-alloyed InGaAs ohmic contacts, thereby increasing $R_D$. 

Silicon Field Emitter Arrays (FEDs) have some deficiencies when used as electron emitters in flat panel displays: high addressing voltages and non-uniform and unstable emission current. Typical FEDs use a series resistor to stabilize the current; however a more efficient approach is the use of a voltage controlled current source such as a MOSFET. In this project, LD-MOSFETs are added in series with Si field emission arrays. The LD-MOSFET is expected to stabilize the current and lower the switch voltage. This makes active matrix FED and other devices requiring smart electron sources feasible. We took advantage of silicon technology because FEAs were fabricated on a silicon substrate. The goal of this project is to demonstrate the integration of silicon MOSFET technology with silicon FEAs.