Low-Power, High-Speed Analog-To-Digital Converters for Ultra-Wideband Application

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Sponsorship: MARCO C2S2, MIT Center for Integrated Circuits and Systems

With the emergence of the Ultra-Wideband (UWB) wireless communication and the general versatility of digital signal processing, wireless systems have demanded higher speed ADC’s. This thesis investigates topologies to reach these higher speeds. In particular, this work will design a 20-giga-sample per second with six effective bits in a 0.18-CMOS technology. The requirement for power efficiency further constrains the design. A time-interleaved architecture is explored as a means to optimize the power dissipation for a given speed (Figure 1). Preliminary design calculations indicate that the optimal total power occurs with massive time interleaving, on the order of several hundred channels. The two main design considerations for such a large parallel system are matching between the channels, and the generation and distribution of the several hundred clock phases. This work looks at various means of performing digital background calibration to account for the mismatches between the ADC’s. Several methods for generating and distributing a large number of clock phases are investigated, including the use of transmission lines. Although this ADC will be applied to the UWB applications, the conclusions and results from this work can apply to general high-speed ADC design or general time-interleaved systems.

Figure 1: Time interleaved ADC topology. Each individual ADC is clocked with a different phase, which time division multiplexes the input signal. Therefore, it allows the overall time-interleaved ADC to operate n times faster than each individual ADC.