Deep Sub-Micron CMOS Analog-To-Digital Conversion for Ultra-Wideband Radio

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Ultra-wideband (UWB) radio uses low signal power spread over a very wide bandwidth and has the potential to transmit at very high data rates over short distances. The minimum FCC-compliant bandwidth of 500MHz occupies 250MHz at DC; Nyquist sampling requires a 500MSample/s analog-to-digital converter (ADC). It has previously been shown that only 4 bits of resolution are sufficient for proper reception in both noise- and interference-limited regimes [1].

A flash ADC is the typical topology used for these specifications. The principal drawback of flash converters is the exponential scaling of comparators versus resolution. Another approach is a time-interleaved successive approximation register (SAR) ADC [2]. A SAR requires only b comparisons, to resolve the b-bit digital output, which can lead to significant savings; however, a SAR suffers from a large input capacitance and high digital complexity. Figure 1 presents a theoretical comparison between flash and SAR energy requirements.

A 500MSample/s, 5b, 6-way time-interleaved SAR converter has been fabricated in 0.18µm CMOS technology. We acknowledge National Semiconductor for providing the fabrication services. A die photograph is shown in Figure 2. We are currently developing new circuit techniques [3] and exploring the usage of a larger number of time-interleaved slices to save energy. A further area of research is using deep sub-micron technology to both reduce the power supply and give substantial savings on the digital energy; these scaled technologies present their own challenges, including larger process variation and component mismatch.

REFERENCES: