A Micropower DSP Architecture for Self-Powered Microsensor Applications

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Distributed microsensor networks consist of hundreds or thousands of individual, miniature sensor nodes. Each node individually monitors the environment and collects data as directed by the user, and the network collaborates as a whole to deliver high-quality observations to a central base station. The large number of nodes in a microsensor network enables high-resolution, multi-dimensional observations and fault-tolerance that are superior to more traditional sensing systems. However, the small size and highly distributed arrangement of the individual sensor nodes make aggressive power management a necessity.

The aim of the µAMPS-2 project is to build a highly integrated, yet versatile sensor system with a strong focus on energy efficiency and agility. Tracking the optimal operating point in the dynamic environments typical for sensor networks requires hardware that can vary clock rates, power supply voltages, and other circuit parameters on-the-fly. The µAMPS-2 architecture consists of a micropower DSP, surrounded by dedicated accelerator blocks for functions performed frequently by each sensor node: FFTs, FIR filters, error correction coding and decoding, and data encryption. A DMA engine efficiently moves data between the DSP and these accelerator blocks. This architecture of highly optimized, on-demand hardware support for energy intensive tasks allows for ultra low-power data manipulation and lowers the processing burden on the DSP core.

An initial implementation of the µAMPS-2 architecture was fabricated in a 0.18µm CMOS technology. We acknowledge National Semiconductor for providing the fabrication services. This implementation included the 16-bit DSP core, an FFT accelerator, and interfaces to custom ADC and radio chips. The fabricated chip operates correctly down to a supply voltage of 0.5V, consuming only 110µW. If the clocks are turned off, the chip can retain its full state using as little as 26µW.

A second-generation µAMPS-2 system is planned, which will improve upon its predecessor by incorporating extensive power-gating, enabling dynamic voltage scaling and shutdown of all individual accelerator cores. The logic will also be designed for sub-threshold operation, resulting in further reduction of signal switching energy.

Figure 1: The µAMPS-2 DSP architecture.
Figure 2: Die photo of first-generation DSP chip.