Spatial filtering circuits used in image processing are often implemented using resistive networks [1][2]. A key element of silicon retinas is a diffusion network comprising an array of lateral and shunt conductances. Spatial filters are also useful for distributed gain control in silicon cochleae [3]. Linear resistive networks using passive resistors are hard to implement in a small area in CMOS-integrated circuits and are not amenable to electronic control. Bi-directional resistive networks can be implemented with MOS transistors whose source and drain terminals are symmetrical and whose gate or bulk voltages may be varied to provide electronic control of the space constant.

Previously proposed current-mode MOS-resistive networks have the following properties: (a) Gate-to-bulk voltages ($V_{GB}$) are not constant and consequently, the space-constant of the network varies with the common mode in an uncontrolled fashion even as the differential voltage between lateral and shunt transistors is fixed; (b) Bulk-to-source voltages ($V_{BS}$) are input-dependent and consequently a MOS-resistive grid exhibits non-linear operation due to the variation of the sub-threshold exponential parameter $\kappa$ with $V_{BS}$. As a result, prior approaches to building resistive grids with MOS transistors resulted in networks whose space-constant varied with the gate-to-bulk voltage and input current intensity. We propose two biasing techniques that alleviate these effects in a current-mode MOS-resistive grid. The first maintains a constant $V_{GB}$ for all transistors in the network regardless of common mode. The second technique suppresses non-linearity due to the body effect induced by varying input currents. Figure 1 shows a photomicrograph of a test-chip fabricated in a 1.5-µm CMOS process. An on-chip capacitive current integration technique is used to obtain precise measurements of sub-threshold currents down to 1fA [4]. Figure 2 shows the measured impulse response of our spatial filter.

REFERENCES: