Reconfigurability is becoming an important factor in the design of systems. FPGAs are extending their application area from system prototyping to custom application implementation but they are much slower and less power-efficient than ASIC systems. We have developed a power- and performance-scalable multi-VDD FPGA. The interconnect overhead for FPGAs is a large fraction of the power and delay, due to the use of programmable switch elements. Fine-grain voltage domains allow low-energy operation in non-critical areas of logic and routing segments. A modified, programmable switch architecture allows long paths to be pipelined to meet critical path timing or, alternatively, allow reduced voltage operation with minimal performance impact.

A better partitioning of non-critical configuration elements to reduce wire lengths produces further reduction in interconnect capacitance. Approximately 70% reduction in the array area is achieved by relocating the switch block and CLB configuration memory to the periphery of the array, resulting in reduced parasitic capacitance on the critical routing wires.

A power-aware place-and-route tool determines which non-critical paths can run at reduced voltage and configures the various domains of the array accordingly. Thus, selecting the appropriate choice of supply voltage for each domain achieves an average 52% improvement in power for the same performance (Figure 1). Low-overhead level converters provide voltage conversion between domains. With these fine-grain controls, the software can make tradeoffs between power and performance and deliver maximum power savings with minimum performance impact. Sub-threshold leakage reduction is also achieved with fine-grain sleep regions that shut down the power supply to inactive circuits. We have designed a 3x3mm chip (Figure 2) using a customized ASIC flow to validate the approach and have developed custom CAD tools to automate the implementation of some of these techniques.

The chip was fabricated in 0.18µm CMOS technology. We acknowledge National Semiconductor for providing the fabrication services.

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**Figure 1:** Benchmark results showing an average improvement of 52% at a VDDH of 1.8V and VDDL of 0.9V.

**Figure 2:** Layout of one logic and switch block tile.