Mixed-signal circuit design has historically been a challenge for several reasons. Parasitic interactions between analog and digital systems on a single die are one such challenge. Switching transients induced by digital circuits inject noise into the common substrate. Analog circuits lack the large noise margins of digital circuits, thus making them susceptible to substrate voltage variations. This problem is exacerbated at higher frequencies as the effectiveness of standard isolation technique diminishes considerably [1]. The effect of substrate noise on the circuits within an IC is typically observed during the testing phase only after the chip has been fabricated. Determination of the substrate noise coupling during the design phase would be extremely beneficial to circuit designers, who can see the effect of the coupling and re-design accordingly before fabrication. This would reduce the turn-around time for circuits and increase the yield of working chips.

We are currently developing a Substrate Noise Analysis Tool (SNAT) that can be used at any point in the design flow. SNAT requires information on the circuit as well as the technology. The circuit information can be as descriptive as the circuit netlist complete with extracted parasitics or as coarse as a verilog netlist. Similarly, the technology information can be as descriptive as a full substrate doping profile with layout or as coarse as knowing only the substrate resistivity and die size.

The tool generates equivalent noise macromodels to describe the digital system. These macromodels are then coupled with a model for the substrate to yield noise information, such as the time domain profile or spectrum at different points on the substrate. The noise that results from shaping by different isolation techniques can also be determined. The resulting substrate noise data can then be used to simulate its effect on various analog circuits. Figure 1 shows the flow of SNAT.

We have verified the results of SNAT with measurements on a digital PLL designed in TI’s 90 nm technology. SNAT yields 12% error in the RMS voltage of the substrate noise when compared to measurements. Figure 2 shows the time domain output of the substrate noise voltage.

REFERENCES: