Comparator-Based Switched Capacitor Circuits (CBSC)

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Traditional analog designs are based on feedback circuits using operational amplifiers (op-amps). In scaled technologies, the design of op-amps becomes extremely challenging. The high gain required for analog feedback systems has traditionally been achieved using cascoded amplifiers. The cascode becomes less attractive at low power supply voltages due to the limits it places on signal swing. In order to achieve the required gain, cascading several stages is required. However, placing a cascade of several amplifiers in feedback compromises the stability and/or frequency response of the system.

A new comparator-based design methodology that eliminates op-amps is proposed. Figure 1 shows two versions of a multiply-by-2 amplifier: (a) the traditional op-amp based design, and (b) the proposed comparator based design. In both circuits, the capacitances $C_{1a}$ and $C_{1b}$ are equal. During phase $\phi_1$, the input voltage is sampled onto capacitors in both circuits. During phase $\phi_2$ of the op-amp based circuit, the op-amp forces node $V_X$ to the common mode voltage ($V_{CM}$). All the charge from $C_{1b}$ is transferred to $C_{1a}$, causing the output to settle to $2V_{IN}$. During phase $\phi_2$ of the comparator-based circuit, the current source charges the output node until the comparator detects that node $V_X$ has reached the common mode voltage ($V_{CM}$). At this moment, the current source is disabled and the charging stops. All charge from $C_{1b}$ has been transferred to $C_{1a}$ and the output is at $2V_{IN}$. In the comparator-based circuit, an additional short phase is required between $\phi_1$ and $\phi_2$ to preset $V_X$ below $V_{CM}$. This phase is omitted from Figure 1.

The comparator that replaces the op-amp determines the accuracy of the proposed method. The required comparator is a continuous-time comparator. The comparator detects the threshold crossing that determines completion of the charge transfer. This event is not synchronized to any system clock. Three factors affect the accuracy of the comparator decision: the offset voltage ($V_{OS}$), delay ($t_d$), and jitter ($\sigma_t$). These effects are illustrated in Figure 2. Offset voltage, due to device mismatch and finite comparator delay, result in signal independent errors that can be corrected. The comparator jitter is a statistical uncertainty in the detection of the threshold crossing due to transistor noise sources. This timing uncertainty can be translated into an equivalent input-referred noise voltage that is superimposed on the comparator threshold voltage. Because of its random nature, noise is a fundamental limitation of accuracy.

Currently, a proof of concept 10-bit, 10-MHz Analog-to-Digital Converter (ADC) is being designed for fabrication in National Semiconductor’s 0.18-µm process. The goal of the design is to demonstrate the methodology of the comparator-based switched capacitor circuit and investigate the accuracy of the comparator.

Figure 1: (a) Traditional op-amp based multiply-by-2 amplifier versus (b) proposed comparator based multiply-by-2 amplifier.

Figure 2: Continuous-time comparator performance metrics.