Analog-Digital Hybrid Signal Processing and Data Conversion

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This work investigates hybrid signal processing, i.e., signal processing with parallel analog and digital signal paths. Applications of hybrid signal processing will focus on filtering and data conversion. The motivation for hybrid processing is to mitigate the traditional kT/C noise constraint in an analog/digital data-sampling interface. Mitigating this constraint will allow higher signal-to-noise ratios (SNR) to be achieved under the low power-supply voltages of scaled CMOS technologies. To accomplish this goal, hybrid signal processing will be used to reduce linearity requirements in continuous-time circuits.

In a sampling circuit, the sampling function introduces kT/C noise. Because continuous-time (CT) sigma-delta (SD) modulators use CT loop filters, the sampling function takes place after signals pass through the loop filter, allowing sampled noise to be shaped and eventually attenuated. Therefore, this project focuses on CT SD modulators.

One difficulty in implementing SD modulators is the implementation of a precise transfer function. Sampled-data circuits such as discrete-time (DT) switched-capacitor filters have precisely controlled transfer functions. In contrast, CT filters require tuning to achieve precise filter characteristics. In general, using tunable components greatly compromises the linearity of the filter.

To alleviate linearity requirements in this tunable filter, hybrid signal processing can be used (Figure 1). In this topology, the anti-aliased input signal is first digitized by a coarse, fast ADC. An analog residue is created using a coarse DAC and a subtractor, analogous to a stage of a pipelined ADC. This small residue passes through the CT filter/SD modulator combination. The output of the coarse ADC passes through a digital filter that matches the SD ADC’s STF and gets combined with the digital output of the SD modulator. In this manner, the amplitude of the SD modulator input is much reduced and so its linearity requirement is relaxed.

It is hypothesized that removing the coarse bits from the input will not affect noise-shaping and signal filtering. Assuming that the coarse DAC is accurate, any quantization errors made by the coarse ADC will be cancelled when the coarse bits are added back at the SD ADC output.

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**Figure 1: Proposed topology**