Digital Implementation and Calibration Technique for High-Speed Continuous-Time Sigma-Delta A/D Converters

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A/D converters are essential building blocks for many applications. In particular, mobile communication devices require low-cost, low-power, and high-performance A/D converters. A sigma-delta A/D converter is often chosen for wireless applications because high resolution and wide bandwidth are achievable by increasing the oversampling ratio and designing the appropriate loop filter. High oversampling ratios are relatively easy to achieve because state-of-the-art CMOS technologies are capable of high frequency operation. However, implementing a low power discrete-time loop filter becomes very challenging as the sampling frequency increases. Therefore, a continuous-time sigma-delta A/D converter is better for a mobile application than its discrete-time counterpart because of its low power consumption.

However, device mismatch is a serious issue for a continuous-time loop filter. Since the mismatch of passive and active elements directly degrades performance, calibration or compensation is necessary to implement a high-resolution and wide-bandwidth A/D converter. In this work, we propose an automatic calibration and compensation technique for a continuous-time loop filter using digital circuits.

The core technique consists of an algorithm that estimates the individual component values of the loop filter. The spectrum of the digital output signal from the sigma-delta converter contains the quantization noise that is shaped by the noise transfer function (NTF). The NTF can be estimated by system identification techniques. A DSP building block is designed to evaluate the parameters of passive and active elements from the estimated NTF. Then, a feedback loop calibrates the passive and active elements. An adaptive digital filter is also used to deal with non-ideality, which cannot be calibrated due to the technology limitations such as finite rising or falling time of signal.

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