Advanced Delay-Locked Loop Architectures for Chip-To-Chip Communication
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A challenging component in high-speed data links is the clock and data recovery circuit (CDR). Two primary functions of a CDR are to extract the clock corresponding to the input data and then to resample the input data. The conventional technique uses a phase-locked loop to tune the frequency and phase of a voltage-controlled oscillator (VCO) to match that of the input data. In some applications, such as chip-to-chip communication, a reference clock that is perfectly matched in frequency to the signal sequence is available. However, the clock and data signals are often mismatched in phase due to different propagation delays on the PC board. In such cases, using a delay-locked loop, as shown in Figure 1, instead of phase-locked loop allows for much simpler design, since only a phase adjustment is necessary [1].

The aim of this research is to develop advanced delay-locked loop architectures for chip-to-chip communication. In order to provide a fine-resolution and wide-range delay, a digital adjustable delay element consisting of a sigma-delta fractional-N frequency synthesizer is proposed, as shown in Figure 2. This new architecture also provides low-sensitivity to process, temperature, and voltage variations compared to conventional techniques using analog adjustable delay elements, as shown in Figure 1. In addition, a new sigma-delta modulator architecture is proposed to provide a compact design with reasonable power dissipation.

![Figure 1: DLL-based data recovery circuit with analog adjustable delay element.](image1)

![Figure 2: Proposed DLL-based data recovery circuit with digital adjustable element.](image2)

REFERENCES: