Fast Offset Compensation of High Speed Limit Amplifiers

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High gain amplifiers require offset compensation to achieve high input sensitivity. Classic offset compensation in wide bandwidth applications with Non-Return to Zero data streams, as encountered in SONET applications, utilizes a feedback path from the output of the amplifier back to its input through an RC low-pass filter [1][2]. Unfortunately, this approach leads to an undesirable tradeoff between offset compensation time and output jitter – a high offset compensation bandwidth has the benefit of achieving fast settling time at the expense of increased data-dependent jitter. Due to this limitation, current approaches suffer from long compensation times, typically greater than 1 ms for SONET OC-48 applications and often require an off-chip capacitor to achieve an acceptably low compensation bandwidth. Although the long compensation times are acceptable for point-to-point links, they pose a severe obstacle for many-to-one links since the speed of the offset compensation loop may determine how quickly one can switch between input channels.

We propose a compensation scheme that leverages a novel CMOS peak detector structure and a variable tap feedback system that dramatically improves the tradeoff between offset compensation settling time and data-dependent jitter due to the offset correction loop. The proposed system enables a 3 orders-of-magnitude improvement in offset compensation time over the classical approach, while maintaining very low data-dependent jitter levels. To demonstrate the technique, a 7-stage resistor-loaded limit amplifier, which utilized the proposed offset compensation technique, was fabricated in National Semiconductor’s 0.18 µm CMOS process. The chip micrograph is shown in Figure 1. Measured results demonstrate offset settling times less than 1 ms while still meeting SONET OC-48 jitter specifications (< 4 ps RMS @ 2.5 Gb/s) (Figure 2).

Figure 1: Chip Micrograph highlighting major system blocks.

Figure 2: Top - Eye diagram of limit amplifier output with 2.5 mVpp PRBS input; Bottom – Step response of control voltage for closed-loop bandwidth of 1 MHz with 5.0 mVpp PRBS input.

REFERENCES: