Realization of the Baseband DSP Core for the Wireless Gigabit LAN

J.K. Tan, C.G. Sodini
Sponsorship: NSF

In the development of wireless standards, the use of the Orthogonal Frequency Division Multiplexing (OFDM) is becoming increasingly pervasive. The Wireless Gigabit LAN (WiGLAN) aims to achieve a high data rate of 1 Gbps through the utilization of OFDM technology in combination with a wide bandwidth of 150 MHz. The high data rate motivates the need to realize the DSP Core in hardware and test its functionality in real-time.

The hardware platform is a Field Programmable Gate Array (FPGA) because it offers programmability and the capability to tradeoff hardware resources for speed. However, even with an FPGA, the implementation of the DSP Core is challenging, because of limited hardware resources and tight real-time requirements. Due to these constraints, the algorithms used in the DSP Core have to be programmed for minimal complexity; algorithms with high complexity take more hardware resources and lengthen the execution time. After the DSP Core has been realized in hardware, 2 PCs are connected to the DSP Core via PCI to perform high-speed transmission.

The goal is to demonstrate a prototype of the WiGLAN’s communication system in which the realized DSP Core will be integrated with the RF Front-End. This test prototype is the primary vehicle for the performance evaluation of the system. The many uses of this prototype include: determining the role of DSP algorithms in mitigating RF imperfections and characterizing the 5-GHz indoor wireless channel.

![Figure 1: Block diagram for the baseband transceiver to be interfaced with the RF Front-End.](image-url)