Modeling and Simulation of Advanced Transistors with Novel Channel Materials

O.M. Nayfeh, D.A. Antoniadis
Sponsorship: MARCO MSD, SRC

Recent experimental results [1] have demonstrated significant mobility enhancement in transistors such as the dual channel heterostructure-on-insulator (HOI). Germanium is optimally incorporated in the channel to provide increase in mobility. The increase in mobility in an HOI structure is due to Germanium's bulk nature, and also from strain effects due to the lattice mismatch between silicon and germanium. In this work, we examine by modeling and simulation, electrostatics and transport of such devices, in order to understand the physical mechanisms that contribute to enhanced mobility as compared to Silicon-On-Insulator counterparts. Moreover, we determine the performance limits of such channel materials for integration in deep sub 45 nm transistors.

Modeling of such advanced devices requires the determination of key electrostatic parameters; either theoretically, or from measurements of experimental structures. These parameters are affected by strain, quantum-mechanical, and high-field effects. Figure 1 shows the Hole density in an HOI structure at a cut through the center of the channel. The silicon cap thickness is 7 nm and the SiGe layer is ~12.5 nm. The gate potential is –1.7 V. Shown is the solution from a Schrödinger/Poisson calculation, and also from the calibration of the Density-Gradient quantum mechanical correction model. Figure 2 shows the respective Gate-Capacitance vs. Gate-Voltage curves. Both plots show good agreement between the two models after calibration.

REFERENCES: