Three-Dimensional Oxidation of Shaped Silicon Surfaces

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As silicon device dimension decreases, a three-dimensional silicon oxidation mechanism becomes more important. The device can no longer be assumed to have one or two dimensions, but all three dimensions have to be taken into account. The objective of this work is to study the three-dimensional silicon thermal oxidation behavior by examining the oxidation sharpening process for forming silicon field emission tips. Field emission arrays (FEAs) have been studied as potential electron sources for a number of vacuum microelectronic device applications. A field emitter is usually a high aspect ratio microstructure (tip height >> tip diameter). It results in a high electrostatic field at the apex when a voltage is applied to a proximate annular electrode.

Three-dimensional thermal oxidation behavior on silicon is examined by studying the oxidation process for forming silicon field emitters. Oxide growth rate on the convex surface of a silicon feature is retarded due to stress. The sidewalls of the silicon features have a slightly higher oxidation rate because the sidewalls have more atomic steps due to their curvature increasing the reaction surface area. The oxidation rate of the top of the silicon post depends on the stress relief from the convex edges and the influx of excess oxidants from the convex edge. Figures 1 and 2 show the transmission electron microscope (TEM) images of the silicon features with different original oxide cap size.

Figure 1: Transmission electron microscope (TEM) image of the silicon feature (original oxide cap size is 1.1 µm) oxidized at 950 °C for 15 hours.

Figure 2: TEM image of the silicon feature (original oxide cap size is 1.8 µm) oxidized at 950 °C for 15 hours.