Pentacene TFT performance is strongly dependent on the morphology of the pentacene semiconductor. Larger grain sizes and hence, fewer grain boundaries, have been linked to improved mobility and on/off ratios \[1,2\]. By modifying the condition of the pentacene growth surface, i.e. the surface of the gate dielectric, pentacene crystallinity and TFT performance may be improved. A more hydrophobic surface is expected to result in better packing of pentacene molecules; Yasuda, et al. reported improved mobility and on/off ratios in pentacene TFTs using more hydrophobic dielectrics \[3\]. In our work, pentacene TFTs were fabricated using parylene, an organic polymer, as gate dielectric. We examined the effects of an ammonium sulfide treatment and a spin-on polystyrene treatment of the parylene prior to pentacene deposition, and compared the performance of TFTs using (a) untreated parylene, (b) ammonium sulfide-treated parylene, and (c) polystyrene-treated parylene.

Contact angle measurements confirmed an increase in surface hydrophobicity after both treatments. Atomic force microscopy (AFM) and optical microscopy using crossed polarizers showed comparable pentacene grain sizes in the untreated and polystyrene-treated samples. Because of increased average surface roughness, pentacene grain size in the ammonium sulfide-treated sample was smallest (Figure 1). Electrical characterization confirms the trend seen in the physical characterization. Field effect mobility, calculated from conventional saturation region FET equations at \( V_{GS} = V_{DS} = -100V \), is significantly poorer in the ammonium-treated device and comparable in the polystyrene and untreated devices (Figure 2). After gate voltage was scaled (to account for different dielectric thicknesses) to obtain the same electric field in each device, the polystyrene-treated device shows the highest mobility. These physical and electrical characterization results demonstrate the importance of the quality of the pentacene growth surface.

![Figure 1: Optical micrographs using crossed-polarizers of pentacene on (a) untreated, (b) ammonium sulfide-treated, and (c) polystyrene-treated parylene. Each image covers a 36.6μm x 25.6μm area. Measured grain sizes are summarized in the table.](image1.png)

![Figure 2: I-V characteristics for (a) control, (b) ammonium sulfide- treated, and (c) polystyrene-treated transistors. The circles plot mobility vs. gate voltage (right axis). The lines show the extraction of threshold voltage from the saturation region, VDS = -100V (left axis).](image2.png)

**REFERENCES:****

