An All-digital, Pulsed-UWB Transmitter in 90-nm CMOS

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A common metric for comparing the performance of energy-constrained wireless radios is energy consumed per bit transmitted. As the maximum data rate is reduced in a typical wireless link, the energy/bit increases due to the increased on-time of the analog electronics. For low data-rate applications such as RFID tags and wireless sensor nodes, the energy/bit of the wireless link is optimized by employing a very high data-rate radio with a low duty-cycle. This radio can be undesirable from a system perspective when considering network latency and baseband processing. Furthermore, finite startup time of the analog electronics limits the minimum energy/bit that can be obtained. Conversely, pulsed ultra-wideband (UWB) radios can exploit the inherent duty-cycled nature of their signaling to overcome the date rate/on-time tradeoff that leads to increased energy/bit in other radios [1]. The pulsed-signaling also makes UWB transmitters well-suited for an all-digital implementation, resulting in energy/bit proportional to $CV_{dd}^2$, which scales with process technology.

The proposed transmitter will simultaneously achieve sub-nJ/bit energy consumption with a data rate variable from 1 kb/s-1 Mb/s. The data rate may be reduced with very little penalty in energy/bit by avoiding the use of any constant-biased analog circuits such as local oscillators.

The transmitter is designed to operate in a custom transceiver architecture that trades off spectral efficiency for total energy/bit. The frequency plan utilizes the 3.1-5.0-GHz UWB band, divided into three non-overlapping channels of 550 MHz each, as shown in Figure 1. Binary pulse-position modulated (PPM) square pulses are generated in the selected channel at a variable pulse-repetition frequency (PRF) of 1 kHz-1 MHz. The spectrum of PPM signals contains spectral lines that reduce the spectral efficiency [2]. Therefore PPM signals are phase scrambled in order to eliminate these lines. Conventional BPSK scrambling requires differential signaling, adding to the complexity and energy consumption of the transmitter. However, spectral lines may be sufficiently reduced by scrambling with a phase delay as shown in Figure 1. This delay can be fully synthesized and requires no analog components, keeping complexity and energy low. Figure 2 shows the transmitter architecture. Pulses are synthesized by combining a variable number of edges of a delay line clocked at the PRF. The center frequency of the pulse is selected by calibrating the delay/stage in the delay line with an off-line digital calibration loop. The digital pulse is amplified by an inverter chain with power gating for gain control and leakage reduction. The transmitter is capable of driving a 50-Ω UWB antenna with 800-mVppk while consuming <1-nJ/bit.

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**REFERENCES**
