An Analog Storage Cell with 5 Electrons/sec Leakage

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Medium-term analog storage offers a compact, accurate, and low-power method of implementing temporary local memory that can be useful in adaptive circuit applications. The performance of these cells is characterized by the sampling accuracy and voltage droop that can be achieved with a fixed level of die area and power. Typically, the droop rate is limited by the OFF state leakage of a single MOS switch. Past low-leakage switch designs have assumed that subthreshold conduction and drain-to-bulk diode leakage dominate other effects [1-2]. However, measurements of MOS leakage in a 1.5-µm CMOS process revealed a third important mechanism that can contribute significant leakage [3]. It was demonstrated that incorporating a novel MOS switch topology into a high-accuracy switched-capacitor storage cell can minimize all of the experimentally observed leakages, achieving 10-aA average leakage in a 1.5-µm process [3]. New experimental data from storage cells fabricated in a 0.5-µm process (see Figures 1 & 2) exhibit 0.8-aA (5e−/sec) average leakage, a 100× reduction over the leading alternative cell in the literature [2]. This implies that with a 1-pF storage capacitor and a 3.3-V supply, this cell can store a 12-bit accurate voltage for 14.5 minutes and an 8-bit accurate voltage for 3.9 hours. The leakage reduction between the 1.5-µm and 0.5-µm implementations appears to be reasonable based on simple scaling arguments [4].

REbERENCES