A Power-efficient Multi-local PLL Clock Distribution

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In recent generations of high-performance microprocessors, the use of phase-locked loops (PLL) for clock distribution has become more common. As microprocessor operating frequencies increase, the relative impact of clock jitter on the performance of the clock distribution network also increases. Because PLLs have the property of attenuating some of the jitter presented at their input, there have been several investigations [1, 2] into the use of multiple PLLs to distribute the clock. However, the conclusions of these investigations have indicated that the marginal cost of power and complexity for additional PLLs has been too great to warrant more than a single PLL.

In this work, we propose a scalable methodology that utilizes multiple PLLs to reduce the picoseconds of jitter per milliwatt of power in the clocking network. A block diagram of the distribution methodology for a single branch is shown in Figure 1. Distributing the global clock at a lower frequency and locally multiplying up the delivered clock can reduce the cost associated with power, shown in Figure 2, while regulating the buffers local to the PLL can offset jitter accumulation in the PLL. By inserting the PLL deeper into the clock distribution network, fewer unregulated repeaters are needed following the PLL resulting in a net reduction in clock jitter.

### Figure 1
The diagram shows the effective change for a given branch of the clock network for the proposed distribution method.

### Figure 2
Plot of the incremental change in power for each PLL inserted versus the number of PLLs inserted into the network.

### REFERENCES
