A Digitally-enhanced Delta-sigma Fractional-N Synthesizer

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Sponsorship: SRC/FCRP C2S2

Recent advances in frequency synthesizer architectures have formed the groundwork for a very exciting and active area of research. On the one hand, the need for a wider-bandwidth fractional-N synthesizer has inspired researchers to develop phase noise cancellation techniques to avoid tradeoffs between noise performance and synthesizer bandwidth [1], as shown in Figure 1. On the other hand, the continuing development of the deep submicron CMOS process has initiated people’s interest in all-digital phase locked loop (PLL) [2], which not only leverages the high-speed digital capability available in a deep submicron process but also avoids the problems those a conventional charge-pump PLL may encounter, such as high variation and leakage current. The work in [2] demonstrated that an all-digital synthesizer can meet GSM specifications, but the need of a strong DSP capability and a complicated VCO structure prevents it from being a simple solution for many applications. In addition, the bandwidth of [2] is ten times lower than that achievable by analog techniques [1]. Therefore, the goal of this research is to find a digital synthesizer solution that not only is simpler than [2] but also can achieve a high bandwidth comparable to the analog approach [1].

The high in-band phase noise due to the quantization noise of the time-to-digital converter (TDC) in [2] limits the PLL bandwidth to roughly 40 kHz. Recently, a new TDC architecture introduced in [3] demonstrated the possibility of first-order noise shaping the TDC quantization noise. This technique shows the potential to achieve <-110 dBc/Hz in-band phase noise, according to simulation results. With such a low in-band noise floor, we are able to extend the PLL loop bandwidth to roughly 400 kHz without violating the GSM mask.

The digital controlled oscillator proposed in [2] requires a large, fine-resolution switched capacitor bank, which is a challenging design. An alternative in [4] combines a digital-to-analog converter (DAC) and a conventional analog LC voltage-controlled oscillator into a DAC-controlled oscillator. However, the resistor-string DAC used in [4], which offers an easy implementation, will not support dynamic element matching techniques (DEM). Applying DEM to remove the resistor mismatching is critical, since the DAC nonlinearity will fold MASH quantization noise to low-frequencies and thereby overwhelm the benefit of our low-phase-noise TDC. Therefore, we modified the resistor-string DAC into another form that enables us to apply DEM technique easily, just as with the design in [4], this DAC does not require an analog buffer or an op-amp.

By combining the techniques stated above, we expect to achieve a 400-kHz bandwidth digitally-enhanced fractional-N synthesizer with a carrier frequency of 3.6 GHz, which is an order of magnitude higher than offered by [2]. Figure 2 illustrates the block diagram of our architecture. Behavior simulation verifies that the proposed architecture can still meet GSM mask even with the high bandwidth.

REFERENCES


