Digital chip clock distribution consumes a major portion of the chip power budget. On-chip jitter and phase noise measurement promises the ability to control the jitter and power consumption in real-time. Current on-chip jitter measurement systems measure either a histogram with fine resolution [1] or transient jitter using a time-to-digital converter (TDC) with coarser resolution [2]. A finer resolution TDC would result in a single circuit that satisfies both purposes.

In a related application space, recent innovations in frequency synthesizers [3] make increased use of digital components including a TDC as a phase detector. The resolution of the TDC sets an upper limit on the bandwidth of the frequency synthesizer. A finer resolution TDC would result in lower in-band phase noise, wider bandwidth, and greater frequency agility.

Our architecture uses dividers and delay stages to present the delay to the digitizer (Figure 1). The remainder of the system is discrete time. Our work has a time resolution below the minimum inverter delay. All signals are full-swing digital signals with no information stored as low-frequency analog voltages to increase immunity to supply noise. The architecture is suitable for digital standard cells, which allows for simple migration as technology scales.

**Figure 1**: A TDC converter architecture. The dividers and the delay chain present edges to the digitizer.

**REFERENCES**

