Low-power CMOS Rectifier Design for RFID Applications

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We have developed a general theory for far-field RF power extraction (or harvesting) systems. Such systems consist of an antenna and impedance-matching network that capture and efficiently transfer radiated RF power to a rectifier that converts it to DC for powering other circuits [1]. We have studied how fundamental physical relationships that link the operating bandwidth and range of such systems are related to technology-dependent quantities like transistor threshold voltage and parasitic capacitances. An important conclusion is that major improvements in rectifier efficiency are possible when advanced CMOS processes are used to fabricate them. The availability of high-Q capacitors and transistors with lower gate resistance, threshold voltage and parasitic capacitances, i.e., higher $f_T$, in such processes proves to be crucial.

We have used our theory to accurately model far-field power extraction systems for passive RFID tags operating at UHF (850-950MHz). Efficient planar antennas, coupled resonator impedance matching networks and low power all-MOS rectifiers fabricated in standard CMOS technologies (0.5µm and 0.18µm) have been individually designed and later combined to form complete power extraction systems. One of our systems was found to have power-up thresholds of 6µW±10% (at 1µW load) and 8.5µW±10% (at 2µW load) while operating around 950MHz, closely matching values predicted by theory (5.2µW and 8µW, respectively). These low values of the power-up threshold allow the operating range of passive RFID tags to be extended without increasing the transmitted power. As far as we know, our experimental results constitute the best performance reported from a far-field power extraction system built in standard CMOS to date.

REFERENCES