The tunneling field-effect transistor (TFET) is interesting as a promising candidate for future complementary metal-oxide-semiconductor (CMOS) technology due to its potential for low-voltage operation. To successfully compete with conventional MOSFETs, it is important to decrease the sub-threshold swing (SS) and improve the drive current to reduce the power requirements. Theoretically, the sub-threshold swing of TFETs could be scaled down to below 60 mV/dec at room temperature due to the band-to-band tunneling (BTBT) mechanism of operation. Optimization of tunneling current is complex since it depends on several parameters such as doping concentration and profile abruptness of the source, gate oxide thickness, and low band-gap material [1]. In this work, planar-heterojunction TFETs with Si/strained SiGe have been fabricated with two different nominal Ge concentrations (40% and 70%) and with gate oxide thicknesses of 2.5 and 3.5 nm. Biasing conditions have been utilized in order to observe the different tunneling injection mechanism such as N-channel TFET (NTFET) and P-channel TFET (PTFET). The measurement has been done in NTFET mode by using an N+ bias ($V_{G}$ > 0) condition and a negative gate bias (see inset of Figure 1). The comparison of NTFET I-V characteristics between 70% Ge and 40% Ge content structures is shown in Figure 1. A device with 70% Ge content displays an improved drive current and SS compared to a 40% Ge NTFET due to the reduction in tunneling barrier width and high mobility. Work is in progress with laser spike annealing (LSA) in order to improve performance by reducing Ge out-diffusion during implant activation. Figure 2 shows the comparison of NTFETs with varying oxide thickness. The device with the thinner gate oxide has improved drive current. This trait is due to the improved coupling of the gate potential to the channel [2].

**REFERENCES**


**FIGURE 1:** Measured transfer characteristics (drain current, $I_{D}$, versus $V_{G}$) for NTFETs with 40% SiGe and 70% SiGe. Increasing Ge content improves the drive current and sub-threshold swing. The inset shows a cross-sectional view of the fabricated TFET and an experimental bias setup condition for creating the NTFET operation mode.

**FIGURE 2:** Measured transfer characteristics (drain current, $I_{D}$, versus $V_{G}$) for NTFETs with 2.5- and 3.5-nm-thick gate oxides.