Pattern Dependent Characterization of Copper Interconnect

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Copper Interconnect Dual Damascene Process

Deposit dielectric stack; Pattern trenches & vias

- Electroplating
  - “Superfill” used to fill narrow trenches and vias
  - Ideally: plated surface nearly flat

- Copper CMP
  - Multistep process to remove bulk copper and barrier metal
  - Ideally: polished surface nearly flat
    - no loss in copper wire thickness
    - flat for next level

Repeat for multiple levels of metal
Copper Interconnect Problems

- Polishing stages: bulk polish, barrier polish, and overpolish

Non-uniform plating

Evolving Surface Profile

CMP

Field Oxide Loss

Dishing

Erosion

Overpolish

CMP Process and Problems
Electroplating/CMP Characterization Methodology

Electroplating Process
- Fixed plating recipe

CMP Process
- Fixed pad, slurry, process settings (pressure, speed, etc)
- Variable polish times

Electroplating/CMP Test Wafers

Model Parameter Extraction
- Calibrated ECD Pattern Dependent Model
- Calibrated Copper Pattern Dependent Model

Plating: Measure step height, array bulge/recess and field copper thickness

CMP: Measure dishing, erosion and field copper thickness

Chip-Level Simulation
- Plating: prediction of step height, array height, copper thickness and local pattern density
- CMP: prediction of clearing time, dishing and erosion, final copper line thicknesses

Product Chip Layout
Outline

■ Background
  ❏ Pattern dependent effects in plating and CMP

■ Copper CMP Characterization
  ❏ Polishing Length Scales
  ❏ Test Structure and Mask Design
    • Single Layer Test Structures and Mask Design
    • Multilevel Test Structures and Mask Design
  ❏ Measurements and Analysis
  ❏ Design Rule Generation
  ❏ Chip Scale Modeling

■ Copper Electroplating Characterization

■ Conclusions
Copper CMP Pattern Dependent Effects

Sample Profilometer Scans

Line width = 1 \( \mu m \)
Line space = 1 \( \mu m \)

Line width = 9 \( \mu m \)
Line space = 1 \( \mu m \)
Polishing Length Scales

- Three Polishing Length Scales:
  - ~2mm range: copper bulk polish
  - ~100µm range: erosion profile
  - ~1µm range: dishing profile

Initial Copper Polish

~100µm Range

SEM Cross Section
(0.5µm wide line)
Dishing and Erosion Test Structures

Isolated Line Array Region

- Line width/line space mark
- 500 mm
- 50 mm
- 1.0/1.0/2.0

Typical erosion profilometry scan

Physical Test Structure

- Profilometry: captures surface height over long scans
- Electrical measurements: extract line thickness by probing

Electrical Test Structure

- 2 mm
- 50 mm
- 2200 mm
- 2160 mm

Electrical Measurement

- ∆V
Dishing/Erosion Array Test Structures

- Three Regions:
  - b) Single loop: isolated line
  - c) Small array: loop with surrounding dummy lines
  - d) Large array: multiple taps along length of the array

- Electrical Sampling:
  - Each tap is a Van der Pauw structure: measure resistance
  - Uniform sampling: e.g. every 100 μm
  - Edge sampling: place more taps near the transition region
Copper Thickness Extraction Procedure

Semiconductor Line

- \( R \) is measured line resistance
- \( R_s (\rho/t) \) is sheet resistance
- \( t \) is the thickness of a line
- \( \rho \) is the resistivity of copper
- \( L \) is the length of a line
- \( W \) is the width of a line.
- \( R_{Cu} \) is resistance due to copper
- \( R_L \) is resistance due to liner
- \( \rho_L \) is the resistivity of liner

\[ R = R_s \times \frac{L}{W} \quad \text{or by re-arranging variables} \quad t = \frac{\rho}{R} \times \frac{L}{W} \]  

\[ R_{Cu} = \frac{\rho_{Cu} \times L}{(T_M - T_L) \times (W - 2T_L)} \quad \text{and} \]

\[ R_L = \frac{\rho_L \times L}{(2T_M \times T_L) + ((W - 2T_L) \times T_L)} \]  

\[ T_M = \frac{\rho_{Cu}}{R} \times \frac{L}{(W - 2T_L) + T_L} \]
Additional Structures

**Slotting**
- 100µm
- Cross Section
  - Cu
  - Oxide Fill

**Area**
- 1000µm
- Top Down View

**Capacitance**
- Top Down View
  - Metal 1 Split Combs
  - Metal 2 Solid Plate
- Cross Sectional View
  - Metal 2
  - Metal 1
Single Layer Mask Designs

- Single-level mask: electrical and physical test structures.
- Key pattern factors: density and pitch and/or linewidth and linespace.
- Structure Interaction: structure size and floor planning.
Single Layer Surface Profiles and Trends

Surface Profiles (in Å)

- **Fine Features**
  - 1.0µm/1.0µm Lw/Ls
  - Dishing
  - Erosion

- **Medium Features**
  - 5.0µm/5.0µm Lw/Ls
  - Dishing
  - Erosion

- **Large Features**
  - 50µm/50µm Lw/Ls
  - Dishing

Isolated Lines → Array Region

Scan Distance in µm
Extracted and Physical Copper Thickness

- 300 sec. Polish Time (~11% Overpolish)
- 270 sec. Polish Time (0% Overpolish)
- 330 sec. Polish Time (~22% Overpolish)

- Good correlation between extracted thickness and physical data.
- Clear trend of total remaining thickness is shown from the electrical data.
Analysis: Dishing and Erosion in Copper CMP

Dishing and Erosion Dependencies on Polish Time and Pitch

- Profilometry surface scan for dishing and oxide thickness measurement for erosion.
- Constant dishing after initial transition for smaller pitch structures.
Multilevel Process Sequence and Pattern Problems

1. M1 Polish

2. M2 Oxide Deposition

3. M2 Cu Deposition

4. M2 Polish
Multilevel Copper CMP Test Mask Design

- Multi-level mask: M1, Via, and M2
  - electrical and physical test structures
- Single level effects: Layout factors on M1 to study creation of topography
  - Density
  - Pitch (Line Width & Line Space)
- Multiple metal level effects: Overlay M2 structures to study topography impact
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M1 Structure Design Space (in $\mu$m): < P2D<50 = Pitch of 2 and Density of 50% >

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* D100 Solid
Multilevel CMP Test Structure Design

- Multi-level mask: M1, Via, and M2 with electrical and physical test structures.
- Layout factors: Line width/line space combinations
- Focus: Multi-level pattern effects
- Overlap structures: direct, half, and dual

Mask Layout
(“SEMATECH 954 Mask”)

Half Overlap Structure

- Metal 1: Blue
- Metal 2: Magenta

Arrays

M1 Bond Pad (Top)

M2 Bond Pad (Top)

M2 Bond Pad (Bottom)

Iso. Lines

20mm
Direct Overlap: Structure

Top Down View

Cross Sectional View

M1 Top Pad

Metal 1

M1 Bottom Pad

Metal 2

M2 Top Pad

M2 Bottom Pad

Oxide

Oxide

Metal 1

Metal 2
Direct Overlap: Data Analysis

M2: Electrically Extracted

Overlap
No Overlap

M2: Surface Scan

M1: Electrically Extracted

As Dep. Oxide Profile

Oxide

Metal 2

Oxide

Metal 1
Multilevel Half Overlap Structure

Top Down View

M1 Top Pad

Metal 1

M1 Bottom Pad

M2 Top Pad

M2 Bottom Pad

Metal 2

Cross Sectional View

As Dep. Oxide Profile

Oxide

Oxide

Metal 2

Metal 1
Half Overlap: Erosion to Erosion

M2: Electrically Extracted

M2: Surface Scan

M1: Electrically Extracted

As Dep. Oxide Profile

Oxide

Oxide

Metal 2

Metal 1
Half Overlap: Dishing to Erosion

M2 Profile (Å)
0.5μm Lw/0.5μm Ls

M1 Profile (Å)
50μm Lw/50μm Ls

Scan Distance (μm)
Half Overlap: Erosion to Dishing/Erosion

M2 Profile (Å)
5μm Lw/5μm Ls

M1 Profile (Å)
1μm Lw/1μm Ls

Scan Distance (µm)

Dark band indicates dishing

Erosion Dominant

No Overlap Region
Over Struct.
Over Oxide

M2 Array

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Dual Overlap: Structure
Dual Overlap: Data Analysis

M2 Electrically Extracted

M2: Surface Scan

M1: Electrically Extracted

M1 Remain. Thick. (µm)

M2 Remain. Thick. (µm)

Iso. Lines

Over Struct.1

Over Struct.2

Ref.

Oxide

As Dep. Oxide Profile

Metal 2

Metal 1

Oxide

M2 Remain. Thick. (µm)

M2 Recess (Å )
Multilevel Electrical Impact: M2 Line Thickness

- Metal 2 thickness (0.5 µm line/space) as function of space from the edge of the metal 1 array (3 µm line/1mm space)

- Change in resistance of a 0.5 µm metal 2 line/space structure at a transition in metal 1 density

Lakshminarayanan et al. (LSI Logic), IITC 2002.
Design Rule Generation

Lakshminarayanan et al. (LSI Logic), IITC 2002.
Modeling of Pattern Effects in Copper CMP

- **Stage 1**: Bulk copper removal
- **Stage 2**: Barrier removal
- **Stage 3**: Over-polish

- **Approach**: Apply density/step-height model to each stage in the copper polish process.

- **“Removal Rate” Diagrams**: Track RR for metal and oxide during each phase.

- **Approximation**: Neglect barrier removal phase.

- Oxide Erosion
- Metal Dishing
Pattern-Density / Step-Height Effects

For large step heights:
- step height reduction goes as $1/pattern-density$

For small step heights (less than the “contact height”):
- height reduction proportional to height
- height decays with time constant $\tau$:
  $$\frac{dH}{dt} = H(t)$$

Calculate *effective density* by averaging local pattern densities over some window/weighting function

Ouma et al., IITC ’98;
Smith et al., CMPMIC ’99
Grillaert et al., CMP-MIC ’98.
Chip-Scale CMP Simulation

Dishing after step two

RMS Error = 155 Å
Outline

■ Background

■ Copper CMP Characterization

■ Copper Electroplating Characterization
  ❏ Definitions
  ❏ Test Structure and Measurement Plan
  ❏ Trend Analysis
  ❏ Chip Scale Modeling
  ❏ Integrated Plating/CMP Chip-Scale Modeling

■ Conclusions
Copper Electroplating Non-Uniformities

- Isolated line and array region are recessed
- Isolated line sticks up and array region is bulged
Electroplating Pattern Dependent Effects

AH: Array Height
SH: Step Height
Measurement Plan and Sample Profile Scan

- Profile scans taken across each line/array structure

- Test Mask
- Step Height (Isolated Line)
- Superfill
- Step Height (Array Line)
- Bulge
- Recess
- Zoom into array
- Profile Scan
- Thickness Measurement
- Isolated Line
- Array Region
- Conformal Fill
Electroplated Profile Trends: Pitch Structures

- **Lw/Ls**
- **Superfill Behavior**
- **Conformal Behavior**
Step Height Data Analysis

Step Height vs. Line Width

- Trends
  - SH depends on line width: near zero or positive (superfill) for small features and becomes more conformal as line width increases

Saturation Length: fill becomes fully conformal and SH = Trench Depth
  - Line width $L_W = 10\mu m$
Array Height Data Analysis

Trends
- Positive (superfill) for small features, and becomes negative (conformal), and saturates to field level as line width increases
- Saturation length: fill becomes fully conformal and $AH = 0\text{Å}$
  - Line width $L_W = 10\text{µm}$
SH and AH vs. Line Space

Trends
- Line space dependency for SH and AH is similar to line width dependency
- Saturation length: similar value is observed for line space
  - Line space $L_S = 10 \mu m$
Transition Length Scale in Electroplating

- Plating depends on local feature (feature scale) and nearest neighbors within 2-5µm range.

**Array Height Profile Scans**

- 0.5µm/0.5µm Array
- 5µm/5µm Array

**Array to Array Transition**

- Sharp Transition 1.5µm/3.5µm Array
- 4.5µm/0.5µm Array

**Superfill**

**Conventional fill**
Semi-Empirical Model for Topography Variation

- Physically Motivated Model Variables:
  - Width, Space, 1/Width, and Width*Space

- Semi-Empirical Model Development
  - Capture both conformal regime and superfill regime in one model frame
  - 1/W^2 and W^2 terms explored as well

- Model Form
  - Array Height:
    \[
    AH = a_E W + b_E W^{-1} + c_E W^{-2} + d_E S + e_E W \times S + \text{Const}_E
    \]

  - Step Height:
    \[
    SH = a_S W + b_S W^{-1} + c_S W^2 + d_S S + e_S W \times S + \text{Const}_S
    \]
The models capture both trends well
- Step Height RMS error = 327 Å
- Array Height RMS error = 424 Å

Model coefficients are calibrated and used for chip-scale simulations
Chip-Scale Simulation Calibration Results

- Simulated over the entire test mask used to calibrate the model
- RMS errors are slightly greater (about 90Å and 10Å more) than fitting RMS errors since distribution values are used
Integration of Electroplating and CMP Models

- Integration is done by feeding forward the simulated result from electroplating to copper CMP simulation.

**Electroplating Simulation:**
- Array Height
- Step Height
- Topography Pattern Density

**CMP model needs:**
- Surface “envelope”:
  - Array Height
  - Step Height
  - Topography Pattern Density

**Prediction of dishing and erosion**
Topography Pattern Density

- Topography density: as-plated surface topography pattern density of raised features
  - Depends on plating characteristics
  - Important as an input for CMP pattern density model
Plating/CMP: Final Dishing

Dishing after step three

RMS Error = 140 Å
Plating CMP: Final Erosion

Erosion after step three
RMS Error = 420 Å
Conclusion

- Electroplating and CMP are Highly Pattern Dependent

- Copper Interconnect Pattern Dependent Characterization
  - Test Structure Design
    - Capture Key Pattern Effects: Isolated vs. Array, Density, Pitch, etc.
    - Three Polishing Length Scales: mm, 100µm, and 1µm Ranges.
  - Mask Design
    - Single layer
    - Multi layer
  - Physical and Electrical Measurements
  - Data Analysis


- Provides Data for Chip-Scale Modeling of Copper Interconnect
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