Analysis of Variation in On-Chip Waveguide
Distribution Schemes and Optical Receiver Circuits

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Karthik Balakrishnan
B.S., Computer Engineering
Georgia Institute of Technology, 2004

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Author

Electrical Engineering and Computer Science
May 19, 2006

Certified by

Duane S. Boning
Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by

Arthur C. Smith
Chairman, Department Committee on Graduate Studies
Electrical Engineering and Computer Science
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ABSTRACT

Recently, optical interconnect has emerged as a possible alternative to electrical interconnect at chip-to-chip and on-chip length scales because of its potential to overcome power, delay, and bandwidth limitations of traditional electrical interconnect. This thesis examines the issues of variation involved in the implementation of a robust on-chip optical signal distribution network. First, the variation within the on-chip waveguide network is analyzed in terms of susceptibility to lithographic uncertainties and refractive index variations. Then, the robustness of an ultrashort pulse-based receiver circuit architecture is analyzed. Some variation sources considered are optical input power variation, load capacitance variation, parasitic capacitive coupling, and power supply noise. Simulation results show that, for both the passive waveguide network and the optical receiver circuit, variation can result in clock skew and jitter, which limit the frequencies at which the distribution network can operate.

The impact of technology scaling on the optical receiver circuit architecture is assessed with respect to variation. The robustness of the optical network is compared with that of an all-electrical signal distribution network. Results indicate, for the optical signal distribution network, that a trade-off exists between power consumption and robustness towards most sources of variation. In addition, the ultrashort pulse-based receiver circuit design demonstrates robustness towards many variation sources in the presence of technology scaling. The existence of variation in reasonable amounts will not obstruct the functionality of the receiver circuit. However, additional measures must be taken to minimize power supply variation and parasitic capacitive coupling, which will have a greater impact on robustness in future technology nodes.

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Title: Professor of Electrical Engineering and Computer Science
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Table of Contents

Chapter 1 Introduction and Motivation for Research _________________________ 12
  1.1 Motivation ___________________________________________________ 12
  1.2 Previous Work _______________________________________________ 13
  1.3 Thesis Organization __________________________________________ 14

Chapter 2 Components of the Optical Signal Distribution Network ____________ 17
  2.1 Mode-locked Laser Sources ______________________________________ 18
  2.2 Optical Amplifiers ____________________________________________ 20
  2.3 Optical Modulators ____________________________________________ 21
  2.4 Passive Optical Components – Waveguides, Splitters and Couplers ________ 22
    2.4.1 Waveguides ____________________________________________ 22
    2.4.2 Splitters ____________________________________________ 23
    2.4.3 Couplers ____________________________________________ 23
  2.5 Photodiodes __________________________________________________ 24
  2.6 Optical Receiver Circuits ________________________________________ 26
  2.7 Clock Skew and Jitter __________________________________________ 27
    2.7.1 Clock Skew ____________________________________________ 28
    2.7.2 Clock Jitter ____________________________________________ 28
  2.8 Summary ____________________________________________________ 29

Chapter 3 Variation in Passive Optical Components __________________________ 31
  3.1 High Transmission Cavity Splitter _________________________________ 31
  3.2 Refractive Index Variation ________________________________________ 32
    3.2.1 Localized Refractive Index Variation _________________________ 33
    3.2.2 Global Refractive Index Variation ____________________________ 35
  3.3 Geometric Variations ____________________________________________ 37
  3.4 Sidewall Roughness _____________________________________________ 39
  3.5 Summary ____________________________________________________ 41

Chapter 4 Optical Receiver Circuit Analysis ________________________________ 44
  4.1 Overview _____________________________________________________ 44
  4.2 Photodiode Details _____________________________________________ 46
  4.3 Critical Areas to Examine ________________________________________ 47
    4.3.1 Optical Input Power Variations ________________________________ 47
    4.3.2 Load Capacitance Variations _________________________________ 48
    4.3.3 Capacitive Coupling and Other Noise-driven Parasitics _________ 48
  4.4 Simulation Setup Parameters ______________________________________ 48
List of Figures

Figure 1-1. Power-delay characteristics for optical and electrical interconnects [1] ........................................ 13
Figure 2-1. Schematic of optical clock distribution scheme [8] ................................................................. 17
Figure 2-2. Diagram of a vertical cavity surface emitting laser (VCSEL) [10] ............................................. 19
Figure 2-3. Diagram of a semiconductor optical amplifier (SOA) [13] ..................................................... 20
Figure 2-4. High transmission cavity [16] (left), Constant bending radius [5] (middle), Star-coupler [17] (right) ......................................................................................................................... 23
Figure 2-5. Diagram of a p-i-n photodiode ............................................................................................... 25
Figure 2-6. Diagram of a traditional optoelectronic receiver circuit .......................................................... 26
Figure 2-7. Diagram of clock skew and jitter in a clock distribution network [8] ...................................... 28
Figure 2-8. Schematic of HTJ T-Junction based on [16] ........................................................................... 31
Figure 3-1. Schematic of HTC T-Junction based on [16] ...................................................................... 31
Figure 3-2. Localized vertical and horizontal effective index variation for HTC splitter. (n=3.2) ............... 33
Figure 3-3. Transmission results for horizontal and vertical local effective index variation in the HTC splitter ................................................................................................................................................... 34
Figure 3-4. Splitting ratio results for the horizontal effective index variation in the HTC splitter ............... 35
Figure 3-5. Global (chip-scale) effective index variation for HTC splitter. (n = 3.2) ............................... 35
Figure 3-6. Transmission results for HTC splitter structure with global refractive index variations ......... 36
Figure 3-7. Schematic of HTC splitter with linear blur features at ten critical areas ............................... 37
Figure 3-8. Transmission results as a function of degree of geometric blurring along various corners of HTC splitter ......................................................................................................................................... 38
Figure 3-9. Sidewall roughness in a slab waveguide of width w and correlation length D, centered at x = 0. .................................................................................................................................................. 39
Figure 3-10. Impact of sidewall roughness on transmission power in a waveguide ................................... 40
Figure 4-1. Ultrashort pulsed receiver circuit architecture [27] .............................................................. 44
Figure 4-2. Equivalent circuit model of a photodiode [23] ..................................................................... 46
Figure 4-3. Sources of variation in ultrashort pulsed optical receiver circuit ........................................... 47
Figure 4-4. Simulation setup for optical input power variation - optical input power variation across the chip, with no mismatch component between the pair of photodiodes ......................................................... 49
Figure 4-5. Simulation setup for optical input power variation - optical input power mismatch between the two photodiodes in the receiver circuit .................................................................................. 50
Figure 4-6. Receiver circuit-scale optical input power variations and resulting skew ............................. 51
Figure 4-7. Simulation setup of load capacitance variation on the performance of the optical receiver circuit ................................................................................................................................................. 54
Figure 4-8. Simulation results of load capacitance variation on the performance of the optical receiver circuit. A skew of 42 ps is the result of a load capacitance variation from 5 fF to 60 fF ........................................................................ 55
Figure 4-9. Simulation setup for capacitive coupling in the optical receiver circuit ................................... 56
Figure 4-10. Simulation results for capacitive coupling in the optical receiver circuit ............................ 57
Figure 4-11. Simulation setup for static power supply variation analysis in the optical receiver circuit .... 58
Figure 4-12. Results of simulation of static power supply variation. A skew of 34 ps is seen from a ±10% variation in the power supply voltage ...................................................................................... 59
Figure 4-13. Circuit-level model used to simulate the impact of dynamic power supply variation on the optical receiver circuit [34] .................................................................................................. 60
Figure 4-14. Results of simulation of self-induced dynamic power supply variation. The observed jitter is less than one picosecond, caused by a 40 mV perturbation of the supply voltage due to parasitic inductances and capacitances .................................................................................................................. 61
Figure 4-15. The clock signal generated by the optical receiver circuit is used to drive an 8 flip-flop pseudorandom sequence generator to determine the effect of dynamic power supply variation ......... 63
Figure 4-16. Results of simulation of total dynamic power supply variation ........................................... 64
Figure 5-1. Receiver circuit-scale optical input power variations and resulting skew in a 65 nm technology. .................................................................................................................................................. 69
Figure 5-2. Simulation results of load capacitance variation on the performance of the optical receiver circuit (65 nm technology node). A skew of 27 ps is the result of a load capacitance variation from 5 fF to 60 fF ........................................................................ 72
Figure 5-3. Results of simulation of static power supply variation for the 65 nm optical receiver circuit. A skew of 42 ps is seen from a ±10% variation in the power supply voltage. ......................................... 73
Figure 5-4. Simulation results of dynamic power supply variation for the 65 nm optical receiver circuit. A 10 ps jitter is seen on the output data line due to the noisy supply voltage and ground signals. .......... 75
Figure 5-5. Simulation results depicting the impact of parasitic capacitive coupling on the output of the optical receiver circuit, using the 65 nm technology node. .......................................................... 76
Figure 6-1. Circuit diagram of electrical H-tree clock distribution scheme. ................................................ 80
Figure 6-2. RLC equivalent circuit model for wires and appropriate numerical values [35]. .................. 81
Figure 6-3. Impact of temperature variation on skew in the 65 nm technology node electrical H-tree clock distribution circuit. ........................................................................................................ 83
Figure 6-4. Impact of temperature variation on skew in the optical receiver circuit, with variation applied only to photodiodes (left) and variation applied to photodiodes and inverter (right). ......................... 84
Figure 6-5. Impact of load capacitance variation on skew in both the electrical and optical 65 nm technology node circuits. ........................................................................................................... 86
Figure 6-6. Impact of dynamic power supply variation on the output of the electrical clock at a leaf node. 87
Figure 6-7. Skew of 44 ps in electrical signal distribution from process variations. .............................. 90
Chapter 1

Introduction and Motivation for Research

This chapter provides motivation for the variation analysis of an on-chip optical signal distribution network. The following sections will describe the interconnect challenges posed by the continuous and aggressive scaling of CMOS technologies. Optical signal distribution networks will be discussed as a potential response to some of these challenges. An outline for the rest of this thesis is provided at the end of the chapter.

1.1 Motivation

Due to the continuous scaling of CMOS technologies and the resulting need for fast, robust and accurate signal propagation, electrical interconnect faces many difficult challenges. Some of these are an increase in wire thickness variation, larger power consumption due to repeater insertion, and an increase in the capacitive and inductive parasitic elements due to the scaling down of wire dimensions. In addition, the need for fast data propagation across chips is becoming too great for electrical interconnect to adequately satisfy with its unfavorable tradeoff curve between speed and power.

A potential alternative to electrical interconnect for on-chip applications is optical interconnect, which allows for the propagation of light through passive optical elements, such as waveguides and splitters, across a chip. The benefits of optical interconnect with respect to the power-delay tradeoff curve are shown in Figure 1-1, which plots the lengths at which optical interconnect will outperform electrical interconnect as technology scales [1]. By 2007, the length at which optical interconnect’s power-delay
product (PDP) is smaller than electrical interconnect is projected to be below the chip edge length (17.6 mm).

![Figure 1-1. Power-delay characteristics for optical and electrical interconnects [1].](image)

In order to determine the viability of optical interconnect, its robustness to different types of variation needs to be analyzed. Temperature gradients, process variations, geometric blurring caused by the fabrication process, as well as circuit-level variations can impact the integrity of the distribution network. Therefore, this thesis will examine an optical signal distribution network and determine its robustness towards these types of variation.

### 1.2 Previous Work

In determining the viability of optical waveguide distribution for on-chip applications, previous work has examined the tradeoffs between electrical and optical interconnect. The International Technology Roadmap for Semiconductors (ITRS) has identified optical clocking as a potential alternative to traditional electrical interconnects.
to overcome its limitations [2]. Some of these limitations include the high power consumption of the buffers along the electrical interconnect lines and the delay along these wires, which are encapsulated in the PDP characteristics. Others include the skew and jitter resulting from process variations and susceptibility to noise. Optical interconnect may have the potential to overcome these limitations. However, many characteristics of on-chip optics still need to be analyzed before concluding the viability of on-chip optical interconnect. In [3], the advantages of optical interconnect are described and the challenges faced in order to implement it are described. Studies have also examined the tradeoffs between optical and electrical interconnect in terms of latency, power consumption, clock skew, cycle time, and other metrics [4]. It was determined that the two most significant challenges in implementing an on-chip optical signal distribution scheme were a) an efficient means of coupling input and output optical power into the circuit, and b) suitable optical-to-electrical signal conversion. In response to these challenges, work has been done to develop robust on-chip systems for on-chip clock distribution [5][6]. Furthermore, preliminary aggregated variation analysis has been conducted on all the relevant components of the optical waveguide system [7]. These components include the waveguide system, the photodetectors, and the MOSFET variations within the receiver circuits.

1.3 Thesis Organization

This thesis is organized in the following manner. Chapter 2 describes the components of an optical signal distribution network as well as the some of their associated sources of variation. Chapter 3 is focused on the analysis of variation in the passive optical components, such as waveguides and splitters. Chapter 4 involves the analysis of
variation in an ultrashort pulse-based optical receiver circuit. The impact of technology scaling on the variation in the optical receiver circuit domain is discussed in Chapter 5. Then, a comparison to a fully electrical distribution system is made in order to determine the tradeoffs involved in using an optical scheme in Chapter 6. Finally, Chapter 7 concludes and provides ideas for future work in this area.
Chapter 2

Components of the Optical Signal Distribution Network

Many components are involved in an optical clock signal distribution network, particularly for clock signal propagation applications. With each of these components, variation plays a role, more significant in some than others, in determining the robustness and viability of the distribution network. A high-level schematic of a possible optical signal distribution scheme is depicted in Figure 2-1. An optical source, possibly an ultrafast pulsed mode-locked laser source or a continuous wave (CW) laser source, is injected into the system.

![Figure 2-1. Schematic of optical clock distribution scheme [8].](image)

Then, the waveguides propagate this optical signal, splitting it at appropriate areas of the chip in order to maximize coverage, up to the receiver circuitry. These receiver circuits then convert the optical pulse into an electrical signal, which in this case, is a clock signal. Then, this electrical clock signal is propagated through wires and buffers to the leaf nodes of the distribution where it can be utilized appropriately by the circuits.
This chapter will provide an overview of the major optical components in this system and briefly describe the sources of variation inherent in each. In addition, Section 2.7 will discuss the notions of skew and jitter as it applies to any clock distribution network.

### 2.1 Mode-locked Laser Sources

Mode-locked laser sources are vital in distributing a low-jitter high-frequency light pulse for both chip-to-chip applications and on-chip applications. The idea behind a mode-locked laser source is that a set of independent modes of a laser, when operating with a fixed phase in between each mode, will periodically constructively interfere to generate a short pulse. This pulse train can then be used for a wide array of applications, such as wavelength division multiplexing or clock and data signal propagation. Recent work has demonstrated the performance of Ti:Sapphire mode-locked lasers which can generate pulses of width 5 fs at a spectral bandwidth of 600-1150 nm [9]. The repetition rate of such pulses is about 100 MHz, while the rms timing jitter is on the order of hundreds of femtoseconds.

The continuous wave (CW) laser source is an alternative to the mode-locked laser source. In a CW laser source, the output signal has constant magnitude and a low peak power. Conversely, in a mode-locked laser source, the output is a pulsed signal with high peak power. Mode-locked lasers have more precise timing, less jitter, and higher peak power than CW lasers, which are all important in building a robust optical clock signal distribution system. Therefore, the robustness of the mode-locked laser source is vital in effectively distribute the optical signal across a chip.

Two types of semiconductor lasers are prominent for generating light pulses. The first is an edge-emitting laser, in which the direction of light propagation is parallel to the
surface of the wafer. More recently, however, surface-emitting lasers have become popular due to their ability to generate low loss, high powered optical pulses. Vertical cavity surface emitting lasers, or VCSELs, are widely used in producing mode-locked laser pulses (as well as continuous wave outputs), and the direction of light propagation is perpendicular to the surface of the wafer. To generate a CW laser using a VCSEL, a short cavity is sufficient, since only one mode needs to resonate within the cavity and be propagated to the output. For a pulsed, mode-locked output, however, the VCSEL cavity must be longer so that the modes of multiple frequencies can resonate and allow the mode-locking effect to occur. A diagram of a VCSEL is shown in Figure 2-2.

![Figure 2-2. Diagram of a vertical cavity surface emitting laser (VCSEL) [10].](image)

A number of variation sources are present in the generation of these optical pulses. One is the rms timing jitter, which represents the root mean square amount of deviation a pulse is offset from its proper location with respect to the specified repetition rate. In addition, optical nonlinearities in the modal cavity such as scattering and the Kerr effect can lead to changes in the shape of the optical pulse, thus resulting in variation in the optical pulse energy [11]. Scattering is an effect that can shift the spectral frequency of an optical pulse towards the longer wavelengths, thereby distorting the optical signal...
(Raman self-frequency shift). The Kerr effect is a phenomenon that results in a change in the refractive index (both with respect to time and with respect to frequency) of the medium in which a pulse travels by the optical intensity of the pulse itself. This slight change in the refractive index results in self-phase modulation, which can alter the shape of the optical pulse.

2.2 Optical Amplifiers

Optical amplifiers are used to boost or restore an optical signal that may have incurred losses over the course of traveling long distances in chip-to-chip, or possibly on-chip, contexts. Another use of an optical amplifier may involve changing the wavelength of an incoming signal, which has proven to be useful in wavelength division multiplexing. For the length scales involving on-chip applications, the semiconductor optical amplifier (SOA) serves to amplify an optical signal by injecting electrical charge into a laser diode-like structure, which then stimulates photons and amplifies the signal. Because of the nonlinear gain function of the SOA and its fast transition time, research has been done to investigate the possibility of using the SOA as part of an all-optical signal distribution network, complete with optical logic gates and optical switching networks [12].

![Diagram of a semiconductor optical amplifier (SOA)](image-url)
The diagram in Figure 2-3 illustrates the high-level function of an SOA. The optical input signal enters through a waveguide. Then, in order to amplify the signal, optical emissions are injected from the top of the structure through the electrical stimulation of a laser diode-like structure. As the amplification process is not perfect, the output signal is emitted from the output facet along with some additive noise components.

These noise components, in addition to high coupling losses, are the most significant drawbacks of the SOA [14]. In order to ensure robust performance, whether it applies to an optical clock signal distribution network or a fully optical computational logic network, the impact of noise and the coupling losses must be examined and mitigated accordingly.

2.3 Optical Modulators

Optical modulators can alter the power, phase, or polarization of the optical signal, thereby encoding data into it. In particular, electro-optic modulators (EOMs) use an electrical input to control the characteristics of the optical signal. When an electric field is applied across the material through which the signal travels, the electro-optic effect induces a change in refractive index, which then results in a phase change on the optical signal. In [15], a semiconductor MOS capacitor is used to induce a phase difference in an optical signal propagating through a silicon waveguide structure, which results in a modulation bandwidth of over 1 GHz. This scheme is significantly different from previous methods of modulation which used a forward-biased p-n junction diode or transistor to inject carriers to create an electric field, which would then induce a phase shift.
Fast optical signal modulation is vital in distributing optical data signals in chip-to-chip as well as on-chip applications while achieving high data rates and bandwidth densities. In terms of variation and robustness, optical modulators can be susceptible to dopant fluctuations, coupling losses, and geometric deviations along critical dimensions. Therefore, in order to enable robust optical signal propagation across long distances while maintaining high data rates, the aforementioned susceptibilities deserve attention.

2.4 Passive Optical Components – Waveguides, Splitters and Couplers

Passive optical components in an on-chip signal distribution scheme are used to send optical signals from a source, such as a mode-locked laser, to an optical receiver circuit. Waveguides, splitters, and couplers are three key components involved in this process.

2.4.1 Waveguides

Waveguides are optical components formed by using different dielectric materials, which compose the core and the cladding, and propagating the light such that it is confined in the core. The variation issues concerning waveguides include refractive index variation of the core or cladding material as a function of location and possibly time, sidewall roughness, and propagation losses over distances and through bends. Research has been done which examines the size and sidewall roughness implications on losses in silicon waveguides and derives a model to capture and quantify the losses caused by them [7]. This work determined that 0.1 dB/cm of loss represents a lower bound on waveguide losses when using an optimal design geometry.
2.4.2 Splitters

![Image of splitters](image)

Figure 2-4. High transmission cavity [16] (left), Constant bending radius [5] (middle), Star-coupler [17] (right).

Waveguide splitters are used, particularly in the context of an H-tree signal distribution system, to split the incoming optical power from a common waveguide branch into two or more output waveguide branches, each with an equal proportion of optical power. Figure 2-4 shows three types of optical splitters, each of which exhibits different characteristics with regards to evenness of splitting ratios and power losses. The variations involved in these splitter structures include geometric blurring along corners as well as refractive index variations, which occur both on a local and global scale.

2.4.3 Couplers

Waveguide couplers are utilized in order to couple an optical signal from a mode-locked laser source such as a VCSEL into a waveguide, or to couple the signal from a waveguide into a photodetector. The key metric by which the effectiveness of a coupler is measured is its coupling efficiency, which represents the percentage of optical power transferred from the input to the output (from a VCSEL to a waveguide, for example). A tradeoff between coupling length and efficiency is a major part of the coupler design process. The coupling length of a coupler is the length of the region of interaction between the input optical pulse and the output optical pulse. Two major types of couplers...
are evanescent couplers [18], in which the interaction between the two surfaces allows for selected modes to move from one area to the other, and volume grating couplers [19], where a series of dielectrics is placed between the input and the output which allows the optical signal to shift from the input medium to the output medium.

As far as variation is concerned, a significant possible source of variation comes from the placement of the coupler. Because the coupling efficiency is closely related to the coupling length, any deviations from either the location or the length of the coupler can reduce the efficiency. Other geometric variables may also be critical, such as the thickness of the layers within the coupling device itself, especially for a volume grating coupler, and the spacing between the waveguide and the coupling device.

2.5 Photodiodes

Photodiode modeling and characterization is important in analyzing the affects of variation on photodetector and receiver circuit performance. In order to accurately model a photodiode, its response must be characterized for both DC input and high-frequency input sources. In addition, information about junction resistances and junction capacitances must be extracted and implemented in the model, and any other components introduced by the uniqueness of its geometry must be included. In [20], PSPICE is used to model and simulate the photoresponse of a photodiode for DC analysis. References [21] and [22] propose photodiode models that encompass the DC responses as well as the high-frequency responses. The main types of photodiodes that are commonly used in optical-to-electrical conversion, depending on the specifications involving bandwidth, power consumption, signal-to-noise ratio, and other factors, are p-i-n and heterojunction photodiodes.
The p-i-n photodiode, shown in Figure 2-5, is used most frequently, due to the ability to tune its characteristics so as to benefit the quantum efficiency and frequency response. The thickness of the intrinsic layer between the p-doped and n-doped regions is directly proportional to the quantum efficiency, while it is inversely proportional to the response speed. Therefore, a p-i-n photodiode can be optimized for either quantum efficiency, fast response speed, or a compromise between the two [23].

![Diagram of a p-i-n photodiode.](image)

The heterojunction photodiode involves combining of different semiconductor materials with different bandgaps in order to optimize a particular feature. In [24], for example, the difference between a homojunction GaN p-i-n photodiode and a heterojunction Al$_{0.12}$Ga$_{0.88}$N photodiode is observed. In this case, the result of implementing the heterojunction was an increase in the quantum efficiency of the photodiode and a decrease in the response speed. Similarly, a heterojunction photodiode can be used in order to achieve the converse effect of increasing the response speed at the expense of quantum efficiency [23]. Thus, this increased level of flexibility allows for designs specifically tailored for large bandwidths, high quantum efficiency, or high response speed. The sources of variation most prominent in the performance of photodiodes include the manufacturing variations which will affect the dimensions of the photodiode, dark current and thermal noise, and random dopant fluctuations.
2.6 Optical Receiver Circuits

The basic components of a traditional optoelectronic receiver circuit are shown in Figure 2-6. The input comes in the form of optical waves, and a photodetector is used to convert this energy into a small electrical current. Then, a transimpedance stage is necessary to change the current into a meaningful voltage, which is then further amplified to be used by the output circuitry that follows.

![Figure 2-6. Diagram of a traditional optoelectronic receiver circuit.](image)

The design of robust optical receiver circuits is critical to the performance of an on-chip optical signal distribution system. Because many of the sources of variability are the most prominent during the optical-to-electrical signal conversion (rather than during the passive waveguiding phase), much work has been done to design a receiver circuit that is not susceptible to variation. In addition to this, the circuits must also be able to operate with small optical input powers in order to alleviate the problem of coupling high-power light onto the chip. In [25], one such low-power receiver circuit design is proposed. Fabricated in 0.5 μm silicon on sapphire CMOS, a power dissipation of 7 mW per channel was achieved with a photodetector capacitance of approximately 500 fF. Alternatively, [26] describes the design and fabrication of a high-speed receiver circuit. Using a 130 nm process, an operation speed up to 8 Gb/s was achieved with a power
dissipation between 10 and 35 mW. Both of these designs use the traditional long-pulsed optical light, and convert that into an electrical signal.

In light of the concerns about variation in receiver circuits, work has also been done in designing a circuit that will be robust to variation and simultaneously require minimal power. The optical pulsing scheme used in [27] is an ultrashort pulse scheme rather than the long-pulsed optical light used in prior designs. The advantages of using this scheme are described in [28], and include the ability to use mode-locked lasers to deliver low-jitter timing-accurate pulses to the distribution system and low-power light distribution.

Previous work focusing on the variation aspects of on-chip receiver circuit designs has also been done [29]. The architecture used for the receiver circuit was the traditional design including the transimpedance amplification phase. In addition, work has also been done in the areas of designing low-jitter, low-skew and variation-tolerant receiver circuits using the aforementioned architecture [8][30][31].

2.7 Clock Skew and Jitter

In an ideal clock distribution network, the clock waveforms located at every leaf node of the distribution have clock edges which occur simultaneously in time. In addition, at a particular leaf node in an ideal clock distribution network, there is no deviation from one cycle to the next in the frequency at which clock edges occur. However, in the presence of variation sources, an ideal clock is impossible to implement. The two main components of non-idealities within a clock distribution network are skew and jitter, which are both discussed in detail in the following sections.
2.7.1 Clock Skew

Clock skew is a fixed difference in the rise and fall times of clock waveforms at two different locations. The top set of waveforms in Figure 2-7 depicts the nature of clock skew. Consider two different locations on the chip, $A$ and $B$. The fixed difference between the rise and fall times of the clocks at $A$ and $B$ is the clock skew between those two locations. In the event of multiple locations, the clock skew is defined to be the difference between the latest and earliest transition times for a single edge. Clock skew can also be separated into rise time skew and fall time skew.

![Clock Skew Diagram](image)

Figure 2-7. Diagram of clock skew and jitter in a clock distribution network [8].

2.7.2 Clock Jitter

Clock jitter represents a time-varying difference between the rise and fall times of the clock edges at a single location. The bottom waveform in Figure 2-7 shows an example of timing jitter at $A$. Since the rising edges of the clock at $A$ do not all occur at the correct time as expected from a fixed and constant frequency, the clock has a jitter component. The jitter is defined as the difference between the latest and earliest transition times of a
clock edge over the course of many cycles. RMS jitter is the root mean square, or standard deviation, of all the differences accumulated over many cycles between the actual transition times and nominal transition times. Like clock skew, jitter can also be separated into rise time jitter and fall time jitter.

2.8 Summary

This chapter discussed the main components of variation in an optical signal distribution network. The optical source, waveguides, photodetectors, and receiver circuits all contribute to the total variation of the distribution system. The importance of this discussion comes from the fact that robust, variation-tolerant optical distribution systems are required if optical interconnect is to replace or augment traditional electrical interconnect on a chip-scale.
Chapter 3

Variation in Passive Optical Components

This chapter discusses the variation involved with optical splitters and waveguides. In the optical signal distribution process, variations can be critical to the overall robustness of the scheme. The first section presents the details of the high transmission cavity splitter. Then, refractive index variations and geometric variations are discussed as they relate to the splitter. Issues of sidewall roughness in straight waveguide segments are analyzed. Finally, the results are summarized and the chapter is concluded.

3.1 High Transmission Cavity Splitter

The high transmission cavity splitter, or HTC splitter, is used as a sample waveguide splitter structure in order to determine the effects of refractive index variation on the light transmission outputs. This T-junction design has been reported by Manolatou et al. [16]. The splitter uses a low loss resonant cavity to redirect the incoming light signal to two output ports which are both rotated 90 degrees from the input port. Crucial to the design is coupling from the input wave to the resonant modes, requiring strong confinement of the electromagnetic fields within the waveguiding structure. This confinement requirement translates to a high index contrast from the waveguide to the cladding region.

![Figure 3-1. Schematic of HTC T-Junction based on [16].](image)
A schematic of the HTC T-junction is shown in Figure 3-1. The optical signal in this schematic enters from the input port, located at the bottom of the diagram, and exits at two output ports, located on the left and right of the diagram. A reduced 2D model is given in [16], with refractive index of the core material at 3.2 and a cladding index of 1.0.

### 3.2 Refractive Index Variation

Refractive index variation can occur both spatially over an area across a chip and temporally on the same part of a chip. When the refractive index of the material is not the same as its nominal value according to the design specifications of the waveguide structures, this can result in transmission losses and splitting losses in these passive structures. Refractive index variation can result from a temperature gradient over the entire chip. The relationship between the refractive index of a material and its temperature is governed by the thermo-optic coefficient. For Si-based optical waveguides, the thermo-optic coefficient is $1.86 \times 10^{-4}$ K$^{-1}$ [32]. There is a linear dependence between the effective refractive index, $n_{\text{eff}}$, and temperature with that slope.

Refractive index variation is pertinent more for two waveguide splitter structures on opposite sides of a chip than within a single splitter itself, because the index is expected to vary little over very short length scales, such as within a few microns. Due to non-negligible chip-scale temperature gradients and impurities in the materials introduced in the fabrication process, the refractive index of the waveguide material can vary enough to cause transmission losses. Analyses of these variations are presented in the following subsections.
3.2.1 Localized Refractive Index Variation

On a local scale, the transmission and the splitting ratio of the high-transmission cavity (HTC) splitter are measured through simulation as a function of the amounts of localized refractive index variation due to possible temperature gradients within that part of the chip. Figure 3-2 depicts the simulation setup as two distinct stages. The splitter located on the left side shows a vertical effective refractive index variation gradient from $n - \Delta n$ at the bottom of the splitting structure to $n + \Delta n$ at the top of the structure. The splitter located on the right side of Figure 3-2 shows a horizontal effective refractive index gradient, also ranging from $n - \Delta n$ to $n + \Delta n$.

![Figure 3-2. Localized vertical and horizontal effective index variation for HTC splitter. (n=3.2).](image)

Figure 3-3 shows the results of transmission loss simulations for both the vertical and horizontal refractive index gradients. In the case of vertical refractive index variations, the transmission losses are examined as $\Delta n$ ranges from 0 to 0.1, and there is a minimal loss of about 0.1% compared to the nominal transmission values. The same holds true for the total transmission losses with horizontal refractive index variation, as there is a drop of less than 0.1% with $\Delta n = 0.1$. 

33
As far as the splitting ratio is concerned, there is a clear linear relationship between the amount of refractive index variation horizontally across the splitter structure and the optical power mismatch between the two output arms of the splitter. When exposed to a purely vertical refractive index gradient, however, there is no change in the uniformity of the split due to the symmetrical nature of the wave propagation direction as compared to the vertical gradient. Therefore, in Figure 3-4, the splitting ratio is plotted as a function of only horizontal refractive index variation (not vertical refractive index variation). The magnitudes of change in the splitting ratio are relatively small (0.9%) when compared to the change of 0.1 in the refractive index.

Figure 3-3. Transmission results for horizontal and vertical local effective index variation in the HTC splitter.
Figure 3-4. Splitting ratio results for the horizontal effective index variation in the HTC splitter.

3.2.2 Global Refractive Index Variation

At the global or chip-scale level, refractive index variation can occur to a higher degree than within a local space, and the impact of this variation can be substantial. Therefore, the analysis of chip-scale refractive index variation is critical in order to determine the robustness of the HTC splitter structure. Figure 3-5 shows the simulation setup for the global variation tests. Many different values for the refractive index of the
material are used in order to simulate the different parts of the chip, whose localized temperatures may cause some deviations in the refractive indices. In each region, a uniform local temperature, and thus refractive index, is considered. Splitter to splitter mismatch on a global scale is now the concern, rather than the variation within the individual splitter.

Figure 3-6 shows a plot of the normalized transmission power versus the change in refractive index on a global scale. These results indicate that, for a change of $\Delta n = 0.1$ in the refractive index, a transmission loss of over 2% is realized. Furthermore, when considering the range of wavelengths from $1.5 \, \mu m < \lambda < 1.6 \, \mu m$, the worst-case transmission drops to almost 96.5%. Clearly, in order to design an efficient and robust optical signal distribution system, the chip-scale temperature distribution must be kept relatively uniform in order to minimize the refractive index variation seen by different splitters on the chip.

![HTC Splitter Transmission: Global Effective Index Variation](image)

**Figure 3-6. Transmission results for HTC splitter structure with global refractive index variations.**
3.3 Geometric Variations

The geometric variations associated with a splitter structure can also have an impact on the characteristics of its performance. Geometric blurring along corners occurs during the lithography and etching processes, which then inhibits the robustness of the splitter. For example, in the high transmission cavity splitter shown in Figure 3-7, ten critical corners can experience geometric blurring due to lithographic processing. These ten areas are categorized into inner corners, outer corners, and v-junction corners as per their concavities. Here, the blurring is modeled as a triangular addition or subtraction from the original HTC splitter geometry. For the inner corners and v-junction, the blurring is modeled with the appending of a triangle to the existing structure at the blurring interface. For the outer corners, it is modeled by the truncation of a triangular segment from the original structure. The variation degree for the geometric blurring is represented by the length of a side of a triangular segment which has either been added or removed from the original HTC splitter structure.

Figure 3-7. Schematic of HTC splitter with linear blur features at ten critical areas.
Simulations conducted by Staker reveal the impact of geometric blurring on the transmission of the HTC splitter [33]. Figure 3-8 plots the transmission from the output arms of the splitter as a function of variation degree. These results indicate that geometric blurring along the inner corners affect the performance of the splitter the most, while blurring along the outer corners is not as problematic. With a variation degree of 120 nm, the transmission loss reaches as much as 10%.

![Summary of Linear Blur Loss for \( \lambda = 1.55 \mu m \)](image)

Figure 3-8. Transmission results as a function of degree of geometric blurring along various corners of HTC splitter.

From these results, it can be concluded that waveguide splitter structures must be designed carefully to be robust to geometrical variation sources incurred during the lithographic process. In an on-chip optical signal distribution network, a signal may be propagated over long distances and pass through many splitter structures. In this case, the effect of blurring in one splitter is compounded many times as the optical signal
propagates from one point on the chip to another. Therefore, well-matched splitting ratios and well as low transmission losses are vital to the robustness of any optical signal distribution network.

3.4 Sidewall Roughness

Sidewall roughness in waveguides, which is caused by uncertainties in the lithographic and fabrication process, can result in propagation losses over long distances. A simulation study was conducted to examine the impact of sidewall roughness on the propagation losses of a straight dielectric slab waveguide. Figure 3-9 illustrates an example of sidewall roughness in a slab waveguide.

![Figure 3-9. Sidewall roughness in a slab waveguide of width $w$ and correlation length $D$, centered at $x = 0$.](image)

The two parameters involved in this analysis are the standard deviation of the waveguide width, $\sigma$, and the correlation length, $D$. The correlation length determines the relative distance across which the waveguide widths are correlated. For example, let $R(d)$ denote an autocorrelation function of the width variance $\sigma^2$ from one point to another point $d$ away. Then,
Sidewall roughness can be separated into two variational components: width variation and position variation. Given a standard deviation $\sigma$, two independent random variables can be constructed to model the sidewall roughness,

$$W \cong N(w, \sigma^2) \text{ and } X \cong N(0,(\sigma/2)^2)$$

where $W$ represents the waveguide width and $X$ represents the coordinate of the center position of the waveguide. The standard deviation of the position is half that of the width so that the two variables are scaled properly and can be compared fairly.

![Transmission Loss vs. Position and Roughness](image)

**Figure 3-10. Impact of sidewall roughness on transmission power in a waveguide.**

For a waveguide of width $w = 0.2 \mu m$ and a correlation length of 50 nm, the results of sidewall roughness analysis simulations are shown in Figure 3-10. The variation in the width of the waveguide, $w$, is denoted as the roughness variation. Similarly, the variations
in the center coordinate of the waveguide, \( x \), is called position variation. The transmission loss through the waveguide increases as the standard deviations of the roughness and position increase, as is to be expected.

In addition, the results show that the sensitivity of the transmission loss to position variation is larger than its sensitivity to width variation. One possible explanation is that the confinement of the mode within the waveguide deteriorates quickly when the slab core itself shifts, but the confinement is still relatively good when the core region is stretched or shrunk, since the electromagnetic waves can still travel in a straight-line path. Work has been done in [5] to develop methods to reduce the sidewall roughness during the fabrication process as well as devise optimal waveguide dimensions to mitigate it.

3.5 Summary

This chapter discussed the effects of refractive index variation on the performance of the high transmission cavity splitter, which can be used as part of an on-chip optical signal distribution system. Results showed that the refractive index variation, resulting from temperature gradients across the chip, can have a significant effect on the optical power losses as well as the splitting ratios. The geometric blurring across corners due to lithographic uncertainties can also affect the transmission efficiency of the splitter structures. The design of an optical clock distribution network must include passive components which are variation tolerant because of their replication across a chip. Since effects of splitting ratios and transmission losses in a splitter are additive, each component must be robust to temperature gradients and geometric blurring. In addition, the impact of sidewall roughness on the propagation losses over long distances in a
waveguide was analyzed. Simulations revealed that the variation in the width of the waveguide, and to a greater extent, variation in the position of the waveguide, cause transmission losses.
Chapter 4

Optical Receiver Circuit Analysis

This chapter describes variation analysis performed on a short-pulse based optical receiver circuit for an on-chip clock distribution application. The first few sections provide an overview of the photodiode modeling and the receiver circuit under consideration. Then, the different sources of variation are described and analyzed in detail. These variation sources are optical input power variation, load capacitance variation, parasitic capacitive coupling, and static and dynamic noise. Finally the chapter is concluded with a summary of the results.

4.1 Overview

The optical receiver circuit which will be the focus of variational analysis here is unlike that designed in previous implementations, in that the input is a fast-pulsed mode-locked optical input rather than a conventional continuous-wave laser [27]. The circuit architecture is shown in Figure 4-1. The reason behind the fast-pulsed lasing scheme is that it allows for low-jitter clock signaling due to the preciseness of the mode-locked
lasers. In addition, this simplified architecture, absent a transimpedance amplification stage or extensive buffering stages, exhibits low capacitance and small area. The low capacitance photodetectors and the minimal amount of circuitry allows for many of these receiver circuits to be fabricated over the span of a chip.

The functionality of this ultrashort pulsed optical receiver circuit is the following. Alternating short pulses are received at each photodiode, delayed by one-half the desired clock period. A pulse on the photodiode connected to the supply voltage will produce a rising edge at the output, while a pulse on the photodiode connected to ground will produce a falling edge at the output. After this clock signal is cleaned up by the static CMOS inverter, a rail-to-rail square wave will be produced at the output, and a load can be driven using this clock signal.

At the optical-electrical interface, a number of specifications are required of both the short pulses and the photodetectors. In order to supply sufficient power to generate a clock signal that can drive an output capacitive load of 15 fF, the input optical power of each pulse must be approximately 430 $\mu$W. In addition, the requirements on the slew rate of the clock and the preciseness of the clock edges require the duration of the input pulses to be less than a picosecond (~100 fs). The wavelength of the optical signal is chosen to be 850 nm, as that is the wavelength for which the quantum efficiency is the highest for the photodiode.

The main characteristics required of the photodiodes are low capacitance and relatively high responsivity. The responsivity is the ratio of photocurrent to input optical power:
To generate a robust gigahertz clock, the capacitance of the photodetectors are to be around 10-15 fF, while exhibiting a responsivity of about 0.5 A/W. Further details of the photodiode are discussed next.

### 4.2 Photodiode Details

A photodiode is a type of photodetector, traditionally operated in reverse bias with a large biasing voltage, which generates electron-hole pairs caused by incident photons [23]. For this work in particular, the type of photodiode used is a p-i-n photodiode, which can be designed specifically to optimize certain parameters such as quantum efficiency by appropriately modifying the depletion thickness. The photodiode model used to conduct simulations is depicted in Figure 4-2.

![Equivalent circuit model of a photodiode](image)

**Figure 4-2. Equivalent circuit model of a photodiode [23].**

$I_p$ is the photocurrent generated as a result of the input optical power. $R_j$ and $C_j$ are the junction resistance and capacitance, respectively. Both are governed by the dimensions of the depletion layer. $R_s$ is the series resistance, and $I_s$ represents a randomly varying current generated by the shot noise, while $I_t$ captures the thermal noise of the photodiode. Finally, $R_L$ and $R_i$ are the external load resistance and the input resistance of an amplifier which may follow the photodiode, respectively.
Table 4-1. Sources of Variation in Ultrashort Pulsed Receiver Circuit.

<table>
<thead>
<tr>
<th>#</th>
<th>Type of Variation</th>
<th>Detailed Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Optical input power variation</td>
<td>Caused by uneven power splits in the passive waveguiding phase</td>
</tr>
<tr>
<td>2</td>
<td>Load capacitance variation</td>
<td>Different loads across the chip will demand different drive strengths of the clock</td>
</tr>
<tr>
<td>3</td>
<td>Parasitic capacitive coupling</td>
<td>Capacitive coupling with a nearby transitioning node can affect the output voltage</td>
</tr>
<tr>
<td>4</td>
<td>Static and dynamic power supply noise</td>
<td>Static and dynamic power supply noise can affect the output voltage by inducing skew, jitter, and transition time variations</td>
</tr>
</tbody>
</table>

4.3 Critical Areas to Examine

The following areas, shown in Figure 4-3, are critical to the robustness of the circuit architecture, and therefore warrant detailed analysis. Table 4-1 describes each source of variation depicted in Figure 4-3.

4.3.1 Optical Input Power Variations

As demonstrated in the previous chapters, accumulated transmission losses and uneven splitting ratios can be caused by geometric blurring in the waveguide splitter structures and refractive index variations. Thus, this variation will result in optical input power variations in the pulse trains at different parts of the chip. In addition, such
variations may also result in an optical input power mismatch between a single pair of photodiodes. The robustness of the circuit architecture against these variations and mismatches will be examined.

4.3.2 Load Capacitance Variations

Because the input power required by the circuit is directly proportional to the capacitive load it must drive, $C_{\text{load}}$ must be the same everywhere across the chip for the receiver circuits to all function in the same way. However, load capacitances vary across the chip because of the way the designer chooses the placement and routing of the cells and wires. The amount of variation which the circuit will properly tolerate is important in determining the robustness of this ultrashort pulsed receiver circuit scheme.

4.3.3 Capacitive Coupling and Other Noise-driven Parasitics

Because of the dynamic nature of the node joined by the pair of photodiodes and the static CMOS inverter, parasitic capacitive coupling can have a detrimental effect on the performance of the receiver circuit. In addition, other noise-driven factors such as static power supply variation and dynamic power supply noise can impact the quality of the output signal. Particularly for clock signal propagation applications, it is important that the output waveform have sharp edges with high slew rates, rail-to-rail swing, and low skew and jitter. Therefore, it becomes necessary to examine the effects of parasitic capacitive coupling and environmental noise on this receiver circuit performance in order to determine its robustness.

4.4 Simulation Setup Parameters

The simulations conducted to determine the impact of variation on the optical receiver circuit are designed using a BSIM 3v3 0.18 μm model with a 1.8 V power
supply. The output clock frequency is 80 MHz, although since the data of interest are clock skew and jitter, the actual frequency itself is not important as long as it is sufficiently small to maintain the accuracy of the skew and jitter results. The junction capacitance $C_j$ of the photodiode is 15 fF, while the series resistance is 5 Ω.

4.5 Optical Input Power Variation

Optical input power variation is important to understand in the context of the robustness of the receiver circuit architecture. The amount of variability tolerated by the receiver circuit at the optical input interface will govern the level of certainty in the correctness at the output interface. Figure 4-4 and Figure 4-5 depict the simulation setup used to determine the effects of variation on the output waveform for the cases of chip-scale variation and mismatch variation, respectively. In Figure 4-5, the mismatch simulations are performed assuming that $I_{\text{pulse}}(\text{top})$ and $I_{\text{pulse}}(\text{bot})$ are independent random variables, drawn from an identical normal distribution.
The ultrashort optical pulse nominally should translate into a current of 432 μA. However, the power of the input pulses is linearly related to the current generated, so a change in the input power will result in a directly proportional change in the current. As shown in Equation 4-2, the photocurrent generated by the photodiode is directly proportional to the optical signal power. Here $\eta$ represents the quantum efficiency of the photodiode; $q$ and $h\nu$ are the elementary charge constant and the energy of a photon, respectively.

$$I_p = \frac{q \eta P_{opt}}{h\nu}$$  \hspace{1cm} (4-2)

The variation associated with optical input power can be characterized into two distinct components. The first is the difference in optical power received at different receiver circuits on the chip. The second involves the mismatch between a pair of photodiodes in the same receiver circuit. This optical power variation can be further dissected into spatial and temporal components.
4.5.1 Optical Input Power Variation: Receiver to Receiver

The result of variation on a chip-scale among receiver circuits at different locations on the chip is clock skew. Because the output signal transition times will differ with varying optical input powers, a clock skew will be induced on the chip. To conduct the simulations necessary to quantify the amount of skew generated, the test setup is shown in Figure 4-4. By changing the magnitude of the current pulse on the photodiodes by an amount $\delta$, the signal at the output of the inverter can be observed, and by aggregating the results, the amount of skew can be determined.

![Figure 4-6. Receiver circuit-scale optical input power variations and resulting skew.](image)

The results are shown in Figure 4-6. The top waveform is the low-to-high transition of the photodiode output resulting from an optical pulse injected at the photodiode connected to the supply voltage. The bottom waveform displays the subsequent high-to-low transition on the output of the inverter. The amount of change in the input pulse on the photodiodes ranged from $\delta = \pm 5\%$ from the mean input current value, $\mu = 432 \, \mu A$, as
shown in the simulation setup diagram in Figure 4-4. The output of the photodiode pair shows a linear relationship between $\delta$ and the final voltage level, which is to be expected since the capacitance being driven is constant. This voltage differential at the photodiode output indirectly causes a variation in the fall times at the inverter output, which creates a skew. According to the waveforms in Figure 4-6, the skew attributed to $\pm5\%$ deviations in optical input power from one receiver circuit to another (in the absence of any mismatch in optical input power between the photodiodes in one particular receiver circuit) is approximately 11 ps. The next section will focus on the issue of optical input power mismatch between two photodiodes within the same receiver circuit.

4.5.2 Optical Input Power Variation: Photodiode Mismatch

Optical input power mismatch between a pair of photodiodes in the same receiver circuit can have two effects. If the mismatch is static and has no time-varying component, the result will be a non-time-varying difference between the rise time and the fall time at the output of the inverter, which in turn will translate into a fixed duty cycle variation. However, if the mismatch varies with time, then the result will be jitter on the signal at the output of the inverter.

To verify these assumptions, a simulation setup is shown in Figure 4-5. The magnitude of the current pulse entering each photodiode is changed, using a Monte Carlo simulation whereby the two optical input power signals are independent and distributed as $N(\mu, \sigma^2)$, for different values of $\sigma$ for each run. For each value of $\sigma/\mu$, 30 simulations are conducted. The results can be interpreted in two different ways. The first interpretation is to consider the variation source to be a time-varying mismatch, and thus observe the results to be a jitter at the output. The second is to consider the variation
source to be a fixed, non-time-varying mismatch and observe the results as a fixed duty cycle variation at the output. The results shown in Table 4-2 quantify the effect of input power mismatch on the jitter of the output clock for the first interpretation as well as the duty cycle variation for the second interpretation. The second column of Table 4-2 shows a linear dependence between the mismatch and the clock jitter is shown. The third column shows the corresponding duty cycle variation which would be present given a 1 GHz clock frequency if the input power mismatch were fixed in time.

Table 4-2. Input power mismatch results.

<table>
<thead>
<tr>
<th>σ/µ</th>
<th>RMS Jitter (ps)</th>
<th>Duty Cycle Variation (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5%</td>
<td>3.61</td>
<td>0.361</td>
</tr>
<tr>
<td>1.0%</td>
<td>7.22</td>
<td>0.722</td>
</tr>
<tr>
<td>1.5%</td>
<td>10.89</td>
<td>1.089</td>
</tr>
<tr>
<td>2.0%</td>
<td>14.61</td>
<td>1.461</td>
</tr>
<tr>
<td>2.5%</td>
<td>18.43</td>
<td>1.843</td>
</tr>
<tr>
<td>3.0%</td>
<td>22.37</td>
<td>2.237</td>
</tr>
<tr>
<td>3.5%</td>
<td>26.51</td>
<td>2.651</td>
</tr>
<tr>
<td>4.0%</td>
<td>30.78</td>
<td>3.078</td>
</tr>
</tbody>
</table>

### 4.6 Load Capacitance Variation

Load capacitance variation is an important consideration in designing any clock distribution network, whether it is electrical or optical. Because different parts of a chip will have different load capacitances which the clock must drive, this variation must be taken into account when designing a clock distribution network for which the clock generated at each output is designed or intended to possess the same drive strength.
Figure 4-7. Simulation setup of load capacitance variation on the performance of the optical receiver circuit.

Figure 4-7 shows the simulation setup for the variation analysis of the load capacitance variation. The capacitive load is modeled as a single capacitor whose value is $C_{\text{load}}$ connected from the output of the receiver circuit to ground. Varying this load capacitance from 5 fF to 60 fF with increments of 5 fF will simulate the different possible values for $C_{\text{load}}$ at different parts of the chip. As a result, the qualitative difference between the output waveforms with different capacitive loads will reveal the impact on the clock signal output of the receiver circuit.

The result of load capacitance variation on the output of the circuit is shown in Figure 4-8. The top waveform is the voltage at the node connected to the output of the photodiode pair. Clearly, the impact of increasing load capacitances on the electrical output is a decrease in the voltage. Because of this decreased drive strength at the input of the inverter, the rise and fall times are altered accordingly, as is shown in the bottom waveform of Figure 4-8.
Figure 4-8. Simulation results of load capacitance variation on the performance of the optical receiver circuit. A skew of 42 ps is the result of a load capacitance variation from 5 fF to 60 fF.

While the smaller values of $C_{load}$ reduce the burden on the inverter and allow for short rise and fall times, an increase in the load capacitance affects the rise and fall times detrimentally. As a result, for the sample case that there is a cross-chip variation in load capacitance from 5 fF to 60 fF, the resulting skew induced on the clock is about 42 ps. Since the minimum clock period that will allow for a fully functional circuit is at least ten times the skew, an upper bound of 2.38 GHz would be placed on the clock frequency based on the skew resulting from this source of variation alone.

4.7 Capacitive Coupling

Noise by way of capacitive coupling on the output node of the photodiode pair can have an impact on the electrical signal at the output of the inverter. Because this node is in a high impedance state for the majority of the time, due to the fact that it is not being driven by any voltage or current, a coupling effect with a nearby transitioning node could
have a detrimental effect on the signal. Figure 4-9 shows the simulation setup used to examine the impact of parasitic capacitive coupling on the photodiode output as well as the inverter output. A node close in proximity to the photodiode output, \( V_{\text{aggressor}} \), makes low-to-high and high-to-low transitions at arbitrary times. The coupling capacitance between the aggressor node and the photodiode output is defined to be \( C_{\text{coup}} \). Then, as the amount of capacitive coupling changes from 0.4 fF to 4.0 fF, the effect on the photodiode output and inverter outputs are observed.

\[
C_{\text{coup}} = [0.4, 0.8, \ldots 3.6, 4.0] \text{ fF}
\]

**Figure 4-9. Simulation setup for capacitive coupling in the optical receiver circuit.**

The effect of the nearby aggressor node \( V_{\text{aggressor}} \) transitions on the output of the photodiode and the output of the inverter is shown in Figure 4-10. Each waveform corresponds to the circuit response at a different value of \( C_{\text{coup}} \), ranging from 0.4 fF to 4.0 fF. During a rising edge on the aggressor node, a percentage of the voltage capacitively couples into the photodiode output node, causing a slight rise in its voltage. Furthermore, because this node is in a high impedance state during all the times except for the optical pulse incidences, the voltage level at the photodiode output is not restored.
after the aggressor node transition is complete. A similar result occurs on the falling edge of the aggressor node, where a dip is seen in the photodiode output as opposed to a rise.

![Figure 4-10. Simulation results for capacitive coupling in the optical receiver circuit.](image)

As far as the inverter output is concerned, a similar degradation occurs as a result of the capacitive coupling. Because the gate voltages of the PMOS and NMOS are reduced (or increased, depending on whether the aggressor node is rising or falling), the inverter voltage dips (or rises) and therefore degrades the clock signal. The clock signal becomes unusable when the parasitic capacitance reaches a value of about 3.0 fF.

In order to mitigate this effect, it may be necessary to isolate the optical receiver circuit from nearby nodes to lessen the parasitic coupling capacitance. In addition, a level restorer could be used to prevent the voltage at the photodiode output from shifting because of the parasitic coupling.

### 4.8 Power Supply Noise

Power supply noise can have a significant impact on the generation of a robust clock or data signal. Just as in a fully electrically distributed network, where capacitive coupling between the power supply lines and data can increase variability in the clock
signal, variations in the power supply can also play a large role in the optical-to-electrical conversion process. Two types of power supply noise are considered for analysis: static power supply variation and dynamic power supply noise.

4.8.1 Static Power Supply Variation

\[
VDD = V_{\text{supply}} + \delta V_{\text{supply}}
\]

\[
\delta = [-0.1, -0.08, \ldots, 0.1]
\]

\[V_{\text{supply}} = 1.8 \text{ V}\]

![Figure 4-11. Simulation setup for static power supply variation analysis in the optical receiver circuit.](image)

Static power supply variation results from a deviation in the nominal power supply value by a constant, non-time-varying amount. This static variation is due to IR drops across long length scales for the power supply grid. Therefore, the value of VDD at one part of the chip may be quite different from its value at another part of the chip. Figure 4-11 shows the framework used to analyze the static power supply variation in the context of the operation of the optical receiver circuit. Different parts of the circuit see different power supplies, differing by a percentage, \(\delta\), of the supply voltage, which in this case is 1.8 V. Then, the impact at the output is analyzed to determine the amounts of skew or other types of distortion that result.
Results of this simulation are shown in Figure 4-12. The top plot shows the output of the photodiode pair, while the bottom plot shows the output of the inverter. Clearly, a skew develops as the power supply varies across the chip by ±10%. In this case, a 34 ps skew is seen, which means that considering this as the only source of variation, the clock period is limited to about 340 ps, corresponding to a frequency of approximately 2.94 GHz. The skew occurs because the amount of total voltage swing is different for each receiver circuit output, due to the different power supply voltage. For example, a receiver circuit operating at a power supply of $0.9 \cdot V_{supply}$ has a shorter “rise time” than a circuit whose operating supply voltage is $1.1 \cdot V_{supply}$. Since the skew is calculated by measuring the difference in time between the earliest and latest signal transition across $0.5 \cdot V_{supply}$, or 0.9 V, there is a clear relationship between static power supply variation and skew.
4.8.2 Dynamic Power Supply Variation

Dynamic power variation in the circuit refers to the change in the voltage of the power supply at one point due to capacitive and inductive parasitics which operate as a function of time. In contrast with the IR drops associated with the static power supply deviations, dynamic variation is caused by parasitic capacitances and inductive noise (also known as L di/dt noise).

Figure 4-13 illustrates a circuit used to model the capacitive and inductive parasitic elements that are the source of dynamic power supply noise. $V_s$ is an ideal DC power supply with no variational components or noise. L4g, R4g, L4v, and R4v represent the inductive and resistive components of the ground and VDD buses, respectively. In deep submicron technologies, the inductance of these rails becomes important enough to require consideration, whereas in previous technologies, the inductive component has had less of an impact than the resistive and capacitive components of the buses. The inverter
shown in Figure 4-13 is a representative circuit which suffers the impact of dynamic power supply variation as a result of the inductors, resistors, and capacitors surrounding it.

The first part of dynamic power supply noise involves self-induced power supply noise, which means that no sources of variation from other circuits are parasitically coupling into the output of the circuit of concern. In other words, the self-induced power supply noise of a circuit represents only the noise caused by its own activity (not the activity of any other circuits).

![Diagram showing photodiode output, inverter output, and supply voltage with notations ~0.3 ps and ~40 mV]

Figure 4-14. Results of simulation of self-induced dynamic power supply variation. The observed jitter is less than one picosecond, caused by a 40 mV perturbation of the supply voltage due to parasitic inductances and capacitances.

Figure 4-14 shows the impact of self-induced dynamic power supply variation on the operation of the optical receiver circuit, assuming that VDD is set by the operation of the supply circuit in Figure 4-13. In the upper two plots of Figure 4-14, the dashed waveform on the left is the photodiode and inverter outputs in the absence of any parasitic
inductances or capacitances. In other words, the left waveforms represent an ideal power supply. To the right of these waveforms is the signal resulting from power supply noise, as modeled in Figure 4-13. Because of the very slight differences in the supply voltage during signal transitions, as shown in the bottom plot, a very small jitter appears at the output of the inverter (0.3 ps). The magnitude of this jitter may be small, but the corresponding 40 mV variation on the power supply may affect nearby signals as well. In addition, as technology scales and feature sizes as well as supply voltages become smaller in magnitude, the parasitic inductances and capacitances may have a larger impact on the optical receiver circuit, especially with increased demands on clock frequency.

The next part of dynamic power supply noise involves the impact of nearby transitioning nodes and their effect on the value of VDD and GND as well as the output node under consideration. Because the optical receiver circuit is likely to share power and ground buses with other circuits, particularly the circuitry which may be driven by the output of the receiver circuit, high-to-low and low-to-high transitions within these nearby areas can cause glitches and variations in the power supply. In turn, these power supply variations can cause the output of the receiver circuit to be distorted.

Figure 4-15 shows the circuit used to test for the impact of full dynamic power supply variation on the optical receiver circuit, rather than simply the self-induced variation. The clock generated by the optical receiver circuit is used to drive a pseudorandom sequence generator of eight stages. Two of the flip-flop Q outputs are XORed together, and this output feeds back into the D input of the first flip-flop. The sequence output can be considered to be the Q output of any one of the flip-flops. The idea behind using this
circuit as a way to determine dynamic power supply variation is the following. Because each flip-flop circuit will share the same supply and ground buses, along with the XOR gate, the many transitions that will occur could potentially have an adverse impact on the clock signal as well as the VDD and GND lines themselves. The power supply variation RLC circuit model described in Figure 4-13 is again used here.

![Figure 4-15](image)

**Figure 4-15.** The clock signal generated by the optical receiver circuit is used to drive an 8 flip-flop pseudorandom sequence generator to determine the effect of dynamic power supply variation.

The results of testing the impact of dynamic and power supply noise on this more complicated circuit are rather interesting. Figure 4-16 shows the impact of VDD and GND variation on the clock signal as well as on the output of the pseudorandom sequence generator. A falling edge on the clock, which is the output of the optical receiver circuit, triggers a low-to-high transition at the output of the sequence generator. Six waveforms are shown: the noisy supply and ground voltage waveforms, the clock waveforms with and without dynamic power supply noise, and the output waveforms with and without dynamic power supply noise. Interestingly, the clock jitter caused by the power supply variations is minimal. However, the clock signal’s fall time (from 1.8 V to 0 V) is impacted adversely, due to the noisy ground voltage being around 100 mV. As
a result of this increase in the fall time of the clock, the effect on the pseudorandom sequence generator output is clear. In addition to the output waveform’s rise time being increased due to the noisy ground signal, the rail-to-rail swing at the output also does not occur due to the VDD noise. Since VDD is around 1.7 V because of the noise, the rise time for the output is impacted even more. In contrast, both the clock and output signals of the noise-free circuits exhibit clear rail-to-rail swings and thus smaller transition times.

![Figure 4-16. Results of simulation of total dynamic power supply variation.](image)

### 4.9 Summary

This chapter detailed the impact of the major sources of variation in ultrashort pulse-based optical receiver circuit architectures. In particular, the main sources of variation considered were the following: a) optical input power variation, both on a chip-scale and a mismatch-scale between two photodiodes in the same receiver circuit; b) chip-scale load capacitance variation; c) parasitic capacitive coupling with nearby transitioning nodes; and d) static and dynamic power supply noise. Results show that the impact of
these sources of variation can contribute to skew and jitter at the output node of the optical receiver circuit, as well as alter the rise and fall times of the transitions which would have an impact on the robustness of the logic following the receiver circuit.

The issues concerning variation in this optical receiver circuit mainly manifest themselves in skew and jitter at the output node. Therefore, the development of techniques to reduce the impact of variation is the key to successful operation at high frequencies. For example, one significant issue in the performance of these circuits is the power supply variation, both static and dynamic. Particularly with the static power supply variation, a 34 ps skew given a ±10% power supply variation is problematic when attempting to achieve operation at high frequencies. Another example involves the parasitic capacitive coupling of a nearby node to the output of the photodiode pair. In this case, the circuit stops functioning correctly only when the parasitic capacitance reaches a threshold of 0.4 fF, which is quite large when considering the length and spacing of coupling which must be present to create that capacitance. More relevant is the challenge of minimizing the capacitive coupling effects to get the maximum benefit of the receiver circuit by employing a rail-to-rail output swing. Of the variation sources examined, none of them, if present in a realistic amount, prevents the receiver circuit from functioning properly altogether. The next chapter will examine whether this holds true in the presence of technology scaling to 65 nm and beyond.
Chapter 5

Impact of Technology Scaling on Optical Receiver Circuit Variation

This chapter describes the impact of technology scaling on the variation of a short-pulse based optical receiver circuit for an on-chip clock distribution application. While the previous chapter discussed the impact of variation in a 0.18 μm technology, this chapter will focus on the effects as they apply to an optical receiver circuit designed using a 65 nm node.

5.1 Overview

The analysis of technology scaling as it applies to variation is important because it leads to an indication of whether or not a given circuit or device will operate properly in future technologies. Therefore, in the process of determining the feasibility of the fast pulse-based optical receiver circuit as device sizes shrink, some predictions and assumptions are made about the technology itself. The 65 nm BSIM4 predictive technology model card is used for the transistors. The photodetector capacitance is assumed to be 2 fF, a reasonable reduction as given by the ITRS roadmap [2], as opposed to the 15 fF photodetectors used in simulating the 0.18 μm case. Furthermore, the values of the inductors and capacitors in the power supply noise model are also modified in order to accurately reflect the technology scaling.

A key component to analyzing the impact of technology scaling is the set of metrics used to evaluate the circuit’s robustness. Skew, jitter, and rise/fall times will be used to quantify the robustness of the output signal, while keeping in mind that the target frequency for a 65 nm process will be much higher than that of a 0.18 μm process. In addition, observing the trends which develop from this analysis may indicate the
scalability of the optical receiver circuit design not just to 65 nm, but also to future technologies.

5.2 Circuit-scale Optical Input Power Variation

The same framework is used for these simulations as in Section 4.5.1. The first portion involves determining the skew caused by receiver-to-receiver variation among various optical input powers across the chip. Given a range of ±5% variation in the input power, a skew of approximately 16 ps is the result. Figure 5-1 shows the waveforms of the photodiode pair output as well as the inverter output. We see that the differences in optical input power result in a smaller (or larger) swing in magnitude of the voltage supplied by the photodetecting process. The difference in this voltage value then alter the rise and fall times at the output of the inverter, which in turn generates a clock skew at the output.

Interestingly, the skew results for the 65 nm simulations (16 ps) is larger than that of the 0.18 μm simulations (10 ps), given the same percentage of input power variation from receiver to receiver in both technologies. Not only is the skew higher for the 65 nm technology simulations, but this effect will be exacerbated by the demands of a high clock frequency. The assumption that the input power variation will vary by the same percentage in both technologies is relatively safe, because the nominal optical input power for a less advanced technology such as 0.18 μm must translate to about 432 μA, while for an advanced technology like 65 nm, the input power requirements are significantly smaller, with the photodetectors only needing to generate about 45 μA of current to drive the inverter which follows it. As a result, the on-chip input power
variations which can be tolerated while still maintaining robust performance becomes very small for future technologies.

![Photodiode output and Inverter output and resulting skew (~16 ps)](image)

Figure 5-1. Receiver circuit-scale optical input power variations and resulting skew in a 65 nm technology.

### 5.3 Optical Input Power Mismatch

Optical input power mismatch involves a difference between the two photodiodes of the same receiver circuit. This difference could either be a static, non-time-varying difference (which results in duty cycle variation) or a dynamic offset which varies with time (which results in jitter). As technology scales, it will be important to minimize the jitter and duty cycle variation that could result from this input power mismatch because increasing amounts of data manipulation need to be performed within one clock cycle. Reliability and robustness are paramount in evaluating the feasibility of the optical receiver circuit design in terms of the optical input power mismatch.
The methodology used in conducting these simulations is identical to that of Section 4.5.2. Given a value of $\sigma/\mu$ for the time-varying mismatch between the two optical input powers, the resulting jitter is determined. Table 5-1 shows the results of the jitter for the 65 nm node optical receiver circuit. For the same $\sigma/\mu$ interpreted as a fixed (e.g. process) variation or mismatch between the two photodiodes, the resulting duty cycle variation on the output is also reported in Table 5-1, assuming an operating frequency of 1 GHz.

**Table 5-1. Input power mismatch results.**

<table>
<thead>
<tr>
<th>$\sigma/\mu$</th>
<th>RMS Jitter in 0.18 $\mu$m (ps)</th>
<th>RMS Jitter in 65 nm (ps)</th>
<th>Duty Cycle Variation in 0.18 $\mu$m (%)</th>
<th>Duty Cycle Variation in 65 nm (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5%</td>
<td>3.61</td>
<td>1.03</td>
<td>.0361</td>
<td>.0103</td>
</tr>
<tr>
<td>1.0%</td>
<td>7.22</td>
<td>2.07</td>
<td>.0722</td>
<td>.0207</td>
</tr>
<tr>
<td>1.5%</td>
<td>10.89</td>
<td>3.73</td>
<td>1.089</td>
<td>.0373</td>
</tr>
<tr>
<td>2.0%</td>
<td>14.61</td>
<td>5.18</td>
<td>1.461</td>
<td>.0518</td>
</tr>
<tr>
<td>2.5%</td>
<td>18.43</td>
<td>6.65</td>
<td>1.843</td>
<td>.0665</td>
</tr>
<tr>
<td>3.0%</td>
<td>22.37</td>
<td>8.17</td>
<td>2.237</td>
<td>.0817</td>
</tr>
<tr>
<td>3.5%</td>
<td>26.51</td>
<td>9.77</td>
<td>2.651</td>
<td>.0977</td>
</tr>
<tr>
<td>4.0%</td>
<td>30.78</td>
<td>11.40</td>
<td>3.078</td>
<td>1.140</td>
</tr>
</tbody>
</table>

In this case, the jitter resulting from the input power mismatch in the 65 nm process is smaller than that resulting from the 0.18 $\mu$m process. There appears to be a clear relationship between the scaling of technology dimension (from 180 nm to 65 nm) and the scaling of RMS jitter, since the jitter values for the 65 nm technology are roughly one-third the values for the 180 nm technology. In other words, reducing the nominal channel length by 3x also reduces the jitter resulting from input power mismatch by 3x. Given further dimension scaling in CMOS technologies into 45 nm and beyond, these
results indicate that the RMS jitter in these circuits is likely to scale along with the technology.

In addition, there appears to be a sub-linear increase in the RMS jitter with respect to $\sigma/\mu$ mismatch for the 65 nm technology node, whereas the increase in RMS jitter is more linear for the 0.18 $\mu$m node. In other words, the slope of RMS jitter versus $\sigma/\mu$ mismatch is higher for the 0.18 $\mu$m node than it is for the 65 nm node. This indicates that input power mismatch will be less of a problem than before with the scaling of technology. This effect may be due to the small transition times of the 65 nm transistors, which effectively make the inverters faster and minimize the effects of any mismatch between the currents seen at the inputs.

5.4 Load Capacitance Variation

The impact of load capacitance variation on the output of the circuit in the 65 nm technology is expected to be lessened due to the enhanced speed and the smaller rise and fall times of the transistors involved in the inverter that follows the photodiode pair. Similar to the simulation setup for the 0.18 $\mu$m case, the load capacitance is varied from 5 fF to 60 fF at different locations on the chip, and the resulting effect on the skew generated is observed. Figure 5-2 shows a plot of the waveforms of both the photodiode output node and the inverter output node.

The results indicate that the skew from the load capacitance variation for the 65 nm technology is 27 ps, which is 15 ps less than the 42 ps which was caused by the same amounts of load capacitance variation in the 0.18 $\mu$m technology circuit. While the skew does improve, it does not quite scale with technology, since it only goes down by approximately 1.6x, while the technology dimension scales by 3x. Therefore, depending
on the desired clock frequency, the scaling of technology can mitigate the impact of load capacitance variation for this particular optical receiver circuit implementation.

![Figure 5-2. Simulation results of load capacitance variation on the performance of the optical receiver circuit (65 nm technology node). A skew of 27 ps is the result of a load capacitance variation from 5 fF to 60 fF.](image)

5.5 Power Supply Variation

Both static and dynamic power supply variation will cause skew and jitter on the output of the optical receiver circuit, as was shown previously in the 0.18 μm circuit. Whether or not the scaling of technology will mitigate these effects, due to the enhanced performance characteristics of the transistors and the decreased photodiode capacitance, or worsened, due to the larger impact of power supply variation with the scaling of supply voltage, must be determined. With this information, future designs of optical receiver circuits can be customized to reduce the detrimental effects of power supply noise as necessary.
5.5.1 Static Power Supply Variation

The impact of static power supply variation for the 65 nm receiver circuit is determined through simulation in the same manner as for the 0.18 μm circuit. Different optical receiver circuits see different power supply voltage values, which vary by as much as ±10%. For this case, the variation is from 0.9 V to 1.1 V. Then, the waveforms at the output of the photodiode, and more importantly, the inverter, is observed to determine the resulting skew.

Figure 5-3. Results of simulation of static power supply variation for the 65 nm optical receiver circuit. A skew of 42 ps is seen from a ±10% variation in the power supply voltage.

Figure 5-3 shows these waveforms, which exhibit a skew of 42 ps given a non time-varying variation of ±10% in the power supply voltage. For the 0.18 μm case, the skew was 34 ps. Therefore, obviously the effect of technology scaling on the impact of static power supply variation is that the variation increases. This occurs because the threshold voltage does not scale with technology. If $V_t$ is 0.2 V for the 0.18 μm technology, it is
likely to be around the same for the 65 nm technology. Therefore, the low-to-high and high-to-low transition times are not improved by virtue of a decrease in the threshold voltage. As a result, when the power supply voltage is scaled down from 1.8 V to 1.0 V, the skew at the output is worsened given the same amounts of variation. However, it should be noted that these simulations do not account for any variation compensation schemes, which can potentially reduce static power supply variation significantly in future technology nodes.

5.5.2 Dynamic Power Supply Variation

Dynamic power supply variation can have an increased impact as technology scales because threshold voltages of devices do not scale very much compared to the supply voltages and device areas. On the other hand, the increased speed of these devices may mitigate the effects of dynamic supply voltage variation. Therefore, it is important to simulate the effects of technology scaling on the operation of the optical receiver circuit.

Using the same framework as in the previous 0.18 μm simulations, the optical receiver circuit is tested in conjunction with a pseudorandom sequence generator (PSR) as the operating circuit which is driven by the clock. In addition, the RLC equivalent circuit model for power supply noise is used to simulate the noise caused by nearby transitioning nodes. Three sets of data are acquired from these simulations: power supply and ground voltage swings, clock voltage waveforms during transitions, and PSR output voltage waveforms during transitions.
Figure 5-4. Simulation results of dynamic power supply variation for the 65 nm optical receiver circuit. A 10 ps jitter is seen on the output data line due to the noisy supply voltage and ground signals.

Figure 5-4 shows the results of these simulations. Just as in the older technology, the clock signal, which is the output of the optical receiver circuit, is not significantly affected in terms of jitter. However, the output of the data circuit, in this case the PSR circuit, is altered in the presence of dynamic noise. The magnitude of this jitter is 10 ps, whereas in the 0.18 μm technology, the jitter is 20 ps. Indeed, the amount of jitter is lessened with the use of the more advanced technology node. However, the normalized amount of reduction may be significantly smaller due to the demand of high clock frequencies for the 65 nm technology process.

5.6 Parasitic Capacitive Coupling

Parasitic capacitive coupling can have a significant impact on the performance and robustness of the optical receiver circuit, as was demonstrated in the previous sections.
Here, the goal is to analyze the impact of technology scaling on the magnitude of the capacitive coupling that occurs between the high impedance output of the photodiode pair and a nearby aggressor node.

Figure 5-5. Simulation results depicting the impact of parasitic capacitive coupling on the output of the optical receiver circuit, using the 65 nm technology node.

Results shown in Figure 5-5 indicate the level of capacitive coupling which can be tolerated by the circuit. The incremental values of the parasitic capacitance range from 0 to 4 fF in steps of 0.4 fF. Therefore, the capacitance at which the photodiode output crosses the threshold voltage of the NMOS or PMOS device that follows it (during a rising edge and falling edge on the photodiode output, respectively) can be determined. This leads to a measure of the maximum capacitance tolerable by the receiver circuit, since the inverter which follows the photodiode pair will not switch from rail-to-rail if its input voltage does not satisfy the threshold voltage requirements. For this circuit, the maximum tolerance of capacitive coupling between the high impedance photodiode
output and a nearby aggressor node is approximately 0.8 fF, whereas for the previous technology the value is 3.0 fF. This increase in susceptibility to noise at 65 nm is a potential concern due to shrinking line spacing and longer lines, which may increase the coupling capacitances. Therefore, additional care must be taken in future technologies to isolate the optical receiver circuits from nearby noise sources.

5.7 Summary

This chapter examined the impact of technology scaling, particularly from a 0.18 μm technology node to a 65 nm technology node, on the robustness of the ultrashort pulse-based optical receiver circuit. Results show that the advanced technology has a mitigating effect on the susceptibility to most sources of variation. However, in most cases, this effect is not strong enough to offset the high clock frequencies and data rates which are generally required of circuits designed in such advanced technology nodes. One notable exception to this is the impact of static power supply variation. Results show that, as technology scales, the magnitude of skew resulting from a 10% variation in the nominal power supply will actually increase (from 34 ps to 42 ps). Therefore, it is especially important for the implementation of this optical receiver circuit in advanced technology nodes to be complemented by the careful design of power supply and ground lines to mitigate this variation.
Chapter 6

Variation Analysis Comparison with Electrical Clock Distribution

This chapter entails the analysis of a fully electrical on-chip clock distribution system in terms of variation and serves to compare it with the previous analysis of the optical clock distribution and receiver circuits. The purpose of this comparison is to determine the strengths and weaknesses of an optical clock distribution approach as compared to an electrical distribution. The electrical distribution is designed and simulated in accordance with the specifications of the 65 nm optical receiver circuit design.

6.1 Overview

The benchmark design for the electrical circuit variation analysis is a 4 mm x 4 mm chip with a 32-node H-tree clock distribution network with sized buffers. In addition, the electrical interconnect is modeled using an RLC equivalent circuit. All simulations were conducted at a temperature of 27 °C at a power supply voltage of 1 V. As in the optical receiver circuits, the variation results will be quantified by skew and jitter amounts at the final output of the clock to be used to drive the logic which follows it. However, in determining the effects of variation on the electrical interconnect performance, a different set of input perturbations will be examined due to the nature of the circuit. For example, while input optical power will not be considered, device and process variations will be analyzed due to the large number of buffering stages in the design. In addition, the absence of any dynamic nodes in this design dictates that parasitic capacitive coupling may not be a large factor in the total variation in terms of skew and jitter, but temperature gradients across the chip could play an important role in the speed and robustness of the electrical buffers through which the clock signal must be carried. Therefore, an aggregate
analysis of the sources of variation in an electrically interconnected clock distribution scheme will be conducted for the purposes of comparison to the optical receiver circuit scheme.

6.2 Electrical Clock Distribution Circuit Details

A diagram of the H-tree clock distribution used for simulation is shown in Figure 6-1. The clock signal enters at the center of the chip. Then, it is distributed through electrical interconnect through a series of buffers which serve to maintain the signal strength. After a series of splits which allow for the clock signal to travel towards different locations on the chip, 32 leaf nodes are created. Theoretically, the same clock signal will arrive simultaneously at each of the leaf nodes, but many sources of variation will contribute to cause clock skew as well as clock jitter.

The wires are modeled using an RLC equivalent, which emphasizes the transmission line characteristics necessary to analyze the distribution scheme in terms of variation.
Figure 6-2 shows the model used as well as the appropriate numerical values for an interconnect line of length 250 μm. All the interconnect wires for the clock distribution scheme are modeled using multiple instances of the 250 μm model.

For a wire of length 250 μm:

\[ R = 10.19 \, \Omega, \]

\[ L = 0.31 \, \text{nH}, \text{ and} \]

\[ C = 27.0 \, \text{fF} \]

The buffers are sized so as to provide maximum drive strength to the clock signal without unnecessarily increasing the inherent loads of the buffers. As the design is in a 65 nm technology, the parameters for the widths of the n- and p-mos transistors are shown in Table 6-1. Each level of buffers has a different size, and the transistors which make up the buffers become smaller as the clock signal approaches the leaf nodes. The sizing of the buffers is derived from a heuristic method which considers the performance of the output leaf node clock at 1 GHz. An initial condition for the buffer sizes is set – the transistor size for the next level of buffers is three times the size of the previous level. Then, the sizes are slightly changed and the clock output is observed until the rise and fall times are less than 10% of the clock period for 1 GHz operation. These transistors are quite large because of the long distances through which the clock signal must be propagated.
This electrical H-tree distribution network is then simulated under certain conditions which introduce variation, and the outputs at the 32 leaf nodes are observed. For example, a chip-scale temperature gradient can be applied, resulting in faster buffers for one path to a leaf node, and slower buffers for another path to a different leaf node. Then, just as a temperature gradient induces refractive index variations and skew in the optical domain, the same temperature gradient will also cause skew in this electrical domain. Other sources such as load capacitance variation, power supply and ground noise, and device variations (threshold voltage, channel length), are also examined.

### Table 6-1. Level of buffer and corresponding transistor widths.

<table>
<thead>
<tr>
<th>Level</th>
<th>( W_p ) (( \mu m ))</th>
<th>( W_n ) (( \mu m ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6.75</td>
<td>3.375</td>
</tr>
<tr>
<td>2</td>
<td>15.75</td>
<td>7.875</td>
</tr>
<tr>
<td>3</td>
<td>20.25</td>
<td>10.125</td>
</tr>
<tr>
<td>4</td>
<td>33.75</td>
<td>16.875</td>
</tr>
</tbody>
</table>

### 6.3 Temperature Variation

Chip-scale temperature gradients can impact the robustness of either an electrical or optical on-chip signal distribution network. In the optical domain, this effect has already been partially examined in Section 3.2, which studies the impact of refractive index variation, which can be caused by temperature gradients, on the performance of waveguide splitters. However, this section will assess the impact of temperature variation on the optical receiver circuit itself and compare it with the corresponding impact on the electrical signal distribution network.
6.3.1 Electrical Distribution Temperature Variation

In the on-chip electrical clock distribution network, the skew resulting from temperature variation is analyzed in the following manner. The chip is divided into two halves: normal temperature and “hot” temperature. In the normal half of the chip, the temperature is exactly 300 K. In the “hot” half of the chip, the temperature of the chip is $300 K + \Delta T$. To determine the skew resulting from this simple temperature gradient, the difference between clock edge arrival times at a node in the normal half and a node in the “hot” half is computed via simulation.

Figure 6-3 shows the falling edge of a clock with values of $\Delta T$ ranging from 5 K to 50 K in increments of 5 K. The waveform of the normal temperature leaf node is also plotted, labeled $\Delta T = 0 K$. The resulting clock skew from this temperature gradient is
34 ps. The next subsection will examine the effects of a temperature gradient on the optical receiver circuit.

6.3.2 Optical Receiver Circuit Temperature Variation

The analysis of temperature variation for the optical receiver circuit is similar to that of the analysis conducted in the previous section for the electrical signal distribution network. Two different optical receiver circuits are considered: one at the nominal temperature of $300 \, K$, and another at an operating temperature of $300 \, K + \Delta T$. The skew is represented by the difference between the arrivals of the rise or fall times at the output of the inverter.

Figure 6-4 shows the results of simulation, with $\Delta T$ ranging from $5 \, K$ to $50 \, K$ in increments of $5 \, K$. For both the left and right waveform pairs, the top waveform displays the voltage at the output of the photodiode pair, while the bottom waveform shows the voltage at the inverter output.
On the left, the skew resulting from temperature variation only in the photodiodes is plotted. In other words, the temperature at which the photodiodes operate is changed by $\Delta T$, but the temperature at which the inverter operates is unperturbed. In this case, the skew is 2.3 ps and comes purely from the voltage differentials at the output of the photodiode. This differential is a result of the change in the thermal noise current, which is directly proportional to the temperature at which the photodiode is operating [23].

On the right side of Figure 6-4, the skew attributed to all the optical receiver components operating at a temperature $300 K + \Delta T$ is plotted. Because the static CMOS inverter which follows the photodiode pair is now also affected, the skew, 21 ps, is much larger than that on the left side of Figure 6-4, and is closer to the 34 ps we observed in the conventional electrical clock distribution case. Combined with the temperature gradient effects in the passive waveguiding, the resulting skew is enough to significantly impact the robustness of the optical clocking scheme if steps are not taken to mitigate the temperature variation.

### 6.4 Load Capacitance Variation: Electrical-Optical Comparison

The impact of load capacitance variation must be considered when comparing the effectiveness of an optical signal distribution scheme with a traditional electrical scheme. Because large amounts of skew could potentially result from varying loads across the chip, the viability of an optical distribution scheme, particularly with the use of an ultrafast pulsed receiver circuit, is dependent upon its robustness in the face of load capacitance variation.

In order to simulate the extent of this effect, the following setup is used. For both the electrical and optical schemes, a nominal mean load capacitance of 15 fF is used. Then,
the actual load capacitances on the chip are distributed as a normal random variable with mean 15 fF, and various standard deviations about that mean.

![Figure 6-5. Impact of load capacitance variation on skew in both the electrical and optical 65 nm technology node circuits.](image)

The simulation results are shown in Figure 6-5. Clearly, in terms of robustness against load capacitance variation, the electrical H-tree distribution performs better than the optical clock distribution. With a small amount of load capacitance variation, the two circuit schemes perform in a similar fashion, but as the variation increases, the slope of the skew increase is significantly larger for the optical circuit than it is for the electrical circuit. This is due to the fact that the load capacitance directly relates to the amount of optical input power required in order to successfully drive that load. Hence, any increase in the load will present a large burden on the photodiode pair to provide the necessary amount of current for a fast transition at the output of the inverter.
Consequently, as Figure 6-5 shows, doubling the amount of optical input power supplied to the photodiode pair reduces the amount of skew generated as a result of the load capacitance variation. Since an increase in the load capacitance will be less significant of a factor due to the ample optical input power (twice what is required for a 15 fF load), the impact on the resulting skew is lessened. This result ties in to the notion of a power consumption tradeoff between electrical and optical signal distributions – an issue which has been examined extensively [36]. For the case of this optical receiver circuit, the electrical clock distribution still seems to handle load capacitance variation more effectively, due to its more favorable relationship between the buffer drive strength and the capacitive loads.

6.5 Power Supply Noise: Electrical-Optical Comparison

The impact of dynamic power supply noise in the electrical signal distribution is analyzed. The same circuit is used to model the power supply noise as in the previous
sections. Figure 6-6 shows the waveforms of the supply and ground voltages at a leaf node, as well as two output clock waveforms – one which is affected by noise, and one which is not. For a 1 V power supply in the 65 nm technology circuit, the simulation results show approximately a 130 mV swing in the VDD line and a 170 mV swing in the GND line. The variations in the supply voltage and ground begin to occur as the clock signal propagates through each stage of buffers and the wires which connect them. The noisy clock, then, is delayed by 40 ps over the clock signal unaffected by noise. As a result, time-varying noise of this nature will result in approximately a 40 ps jitter at a particular output, depending on the amount of noise present at the time of the clock transition, which is difficult to calculate in a deterministic manner.

Unlike the optical receiver circuit scheme, where the data outputs of the pseudorandom sequence generator are affected more adversely than the clock itself, the electrical H-tree distribution scheme generates a clock which can be affected significantly by dynamic power supply noise. This is due to the pulse-based nature of the optical receiver circuit and the consequent charging and discharging of the gate to the inverter, which is relatively independent of power supply noise compared to a buffered electrical line of static CMOS inverters.

6.6 Process Variations

Process variations tend to play a larger role in determining the robustness of an electrical signal distribution network than an optical one because of the variations associated with both the long metal interconnect lines and the buffers used to strengthen the signal as it travels over long distances. Therefore, it becomes necessary to evaluate the performance of the electrical distribution network with process variations, even if it
may be approximate, to provide a better perspective in the comparison between the optical and electrical distribution networks. The following subsections will describe the results of process variation simulations for both the electrical and optical clock signal distribution networks.

6.6.1 Process Variations in the Electrical Clock Distribution

The following elements of process variation are considered for these electrical signal distribution simulations: threshold voltage, channel length, and metal wire resistance and capacitance.

Table 6-2. Process Variation Inputs: Electrical Distribution

<table>
<thead>
<tr>
<th>Variation Source</th>
<th>Amount of Variation</th>
<th>Skew (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold Voltage</td>
<td>$V_{tn} = -V_{tp} = 0.11\text{V}, 0.135\text{V}, 0.15\text{V}$</td>
<td>max – min = 23.1</td>
</tr>
<tr>
<td>Channel Length</td>
<td>$3\sigma/\mu = 10%$</td>
<td>$3\sigma = 29.8$</td>
</tr>
<tr>
<td>Metal Resistance &amp; Capacitance</td>
<td>$3\sigma_{R}/\mu_{R} = 5%, 3\sigma_{C}/\mu_{C} = 5%$</td>
<td>$3\sigma = 1.1$</td>
</tr>
<tr>
<td>Total</td>
<td>N/A</td>
<td>max – min = <strong>44.3</strong></td>
</tr>
</tbody>
</table>

Table 6-2 shows the input sources of variation along with the way in which each of them is altered to determine the resulting skew among the signals at the leaf nodes of the network. For each simulation run, the threshold voltage of each buffer along the paths is selected independently and randomly among three values which span a range of 40 mV. The channel length of each device is sampled from a normal distribution with $3\sigma$ equal to 10% of the nominal channel length. The metal resistance and capacitances are also selected in the same manner, except with $3\sigma$ equal to 5% of the mean. Thirty runs are performed for each set of variation sources. First, the skew which results from each of the
variation sources by itself is determined. The skew resulting from $V_t$ variation is represented by the difference between the latest and earliest clock edges at the output (max-min skew). For the channel length variation and metal line thickness variation, the skew is represented as a zero-mean random variable, whose $3\sigma$ is shown in Table 6-2. The aggregate skew, represented as max-min skew, is determined by observing the combined effect (the min to max deviation across thirty simulations) of all the process variations on the output of the electrical signal distribution network by conducting separate aggregate simulations.

![Figure 6-7. Skew of 44 ps in electrical signal distribution from process variations.](image)

The waveform depicting the skew resulting from the aggregated process variations is shown in Figure 6-7. Though some approximations are made in the formation of the input process variation random variables, such as independence among devices and estimates of the actual deviations in the process, this analysis serves its purpose of isolating the key
sources of variation in an electrical signal distribution network as opposed to an optical
distribution. Next, the impact of process variations in the optical clock distribution will
be analyzed.

6.6.2 Process Variations in the Optical Clock Distribution

In the optical clock signal distribution, the static CMOS inverter which follows the
photodiode pair in the receiver circuit will be susceptible to process variations such as
threshold voltage variations and channel length variations. In this analysis, the amount of
skew resulting from each these variation sources is measured through simulations. The
input parameters are the same for these simulations as for the electrical clock distribution
simulations discussed in Section 6.6.1. The input variation source that represents
electrical interconnect thickness variation is not necessary for this analysis because no
signals in the optical signal distribution scheme are transmitted over long distances
through electrical interconnect.

Table 6-3. Process Variation Inputs: Optical Distribution

<table>
<thead>
<tr>
<th>Variation Source</th>
<th>Amount of Variation</th>
<th>Skew (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold Voltage</td>
<td>$V_{tn} = -V_{tp} = 0.11V, 0.135V, 0.15V$</td>
<td>max – min = 18</td>
</tr>
<tr>
<td>Channel Length</td>
<td>$3\sigma/\mu = 10%$</td>
<td>$3\sigma = 25.9$</td>
</tr>
<tr>
<td>Total</td>
<td>N/A</td>
<td>max – min = 37</td>
</tr>
</tbody>
</table>

The simulation setup is the following. For each run, the threshold voltage for the pair
of devices (NMOS and PMOS in the inverter) is chosen randomly from the three values
listed in Table 6-3, with each choice equally likely, and $V_{tn}$ is always equal to $-V_{tp}$ for the
NMOS and PMOS devices in the inverter. For each run, the channel length for the pair of
devices is chosen from a normal distribution whose $3\sigma/\mu = 10\%$, with $\mu = 65$ nm. Both devices in the pair have the same channel length for that run. The total simulation consists of 30 runs.

Table 6-3 displays the simulation results for threshold voltage variation, channel length variation, and combined variation. The difference between the latest and earliest arrival times of a clock edge is 18 ps when the threshold variation source is applied to the CMOS inverter in the receiver circuit. For the channel length variation of $3\sigma/\mu = 10\%$, the corresponding $3\sigma$ on the clock skew is 25.9 ps, where the skew is considered to be a zero-mean random variable. When the two sources of variation are combined, the \textit{max-min} skew (across the 30 simulations) is 37 ps. All three of these skew results are less than the skew from the electrical signal distribution network, but the values still appear to be quite high, considering the small amount of electrical devices present in the optical receiver circuit architecture.

\textbf{6.7 Summary}

This chapter introduced the analysis of a fully electrical H-tree distribution scheme for the purposes of comparison to the optical distribution system. The similarities and differences among the relevant sources of variation and each of their impacts were discussed. Process variations such as threshold voltage, channel length, and metal width and thickness variation play a significant role in determining the robustness of an on-chip electrical signal distribution network. Temperature gradients play an important role in shaping the viability of both optical and electrical signal distribution networks. In addition, the robustness of the optical scheme also characterized to a degree by threshold voltage and channel length variations. However, it is also characterized mostly by
geometric blurring due to fabrication, waveguide sidewall roughness, and refractive index variation.

Results revealed that the impact of load capacitance variation on the optical signal network is much more prevalent than in the electrical scheme. In addition, the power supply variation affects the two networks in different ways, but both generate a roughly equal amount of skew and jitter. Overall, in terms of variation, there appears to be no clear advantage of using one signal distribution scheme as opposed to the other due to the numerous sources of variation which affect the robustness, of which only a subset are common to both schemes.
Chapter 7

Conclusions and Future Work

This thesis explores the possibility of optical interconnect as an alternative to traditional electrical interconnect in terms of robustness. Because variability is becoming an increasingly important issue with the scaling of technology, an optical interconnect based signal distribution network must be analyzed in terms of variation. This chapter will summarize the contributions of this thesis and present ideas for future work and exploration.

7.1 Contributions

The first contribution of this thesis is the study of variation sources in the passive optical elements which compose the distribution network. Refractive index variation, waveguide sidewall roughness, and geometric blurring are explored to determine their effects on the robustness of the waveguiding scheme. Results show that the waveguide roughness can have a significant impact on the propagation of an optical signal over chip-scale lengths. In addition, care must be taken to minimize the chip-scale temperature gradient, which can adversely affect the splitting ratios of waveguide splitters by as much as 2.5%. Compounded many times through multiple splitter structures over the course of optical signal propagation, the effects of refractive index variation are significant.

The next contribution is the variation analysis of a fast-pulsed based optical receiver circuit, chosen in particular because of its advantages over other optical receiver circuits in minimizing jitter and power consumption. Results indicate that optical input power variation, capacitive coupling, load capacitance variation, and power supply noise can present significant roadblocks to the robust operation of the circuit.
The impact of technology scaling on the variation showed that most of the variation sources become more significant with scaling in the optical receiver circuit domain, just as in the electrical domain. This is mostly due to the presence of the static CMOS inverter which serves as a clean-up buffer for the photodiode output. Threshold voltage, channel length variation, and temperature gradients have a significant impact on the robustness of the architecture. In addition, as technology scales further into 45 nm and beyond, it appears that issues such as power supply variation, parasitic capacitive coupling, and process variation will impose a limit on the robustness of an optical signal distribution scheme.

Finally, a comparison to a traditional electrical on-chip signal distribution scheme at 65 nm revealed that the optical signaling system is more susceptible to load capacitance variation and equally susceptible to CMOS-related process variations. Overall, the on-chip optical signal distribution scheme has some promising features, such as a favorable power-delay product and potential for high bandwidth density, which may allow it to replace long electrical wires on a chip. However, just as issues such as temperature gradients, process variations, and load capacitance variations tend to cause skew and jitter in an electrical distribution network, these effects are not substantially mitigated by an optical signal distribution network based on an ultrashort-pulsed optical receiver circuit. With that said, it remains to be seen the measures which can be taken to limit the impact of variation both in the passive and active optical components without significantly deterring from the potential benefits of optical signaling.
7.2 Future Work

Numerous areas can be explored to discover more about the possibility of optical interconnect as an alternative to electrical interconnect at future scaled technology nodes. In particular, it will become necessary to efficiently measure the variability of a proposed signal distribution scheme in the optical domain. If this can be done, proper modifications can be made to increase the robustness of the clock distribution network. Both the passive components, such as the waveguides, splitters, and couplers, and the active components, such as the optical receiver circuits themselves, must be characterized for the purposes of gathering useful information about the underlying sources of variation and their respective impacts on the performance of the system. Along the same lines, it may also be beneficial to develop analytical or physical models to capture the effects of different sources of variation in the optical domain.

Another area of possible exploration involves active deskewing mechanisms in the optical domain. Although effort has been placed in developing high efficiency, high-bandwidth waveguide structures, it may also become necessary to explore possible schemes to compensate for any bit error or clock skew accumulations because of the relatively long distances over which the optical signals propagate. Such approaches have proven effective in electrical clock distribution [37], and are an important direction for study in the optical approach.

7.3 Summary

This thesis analyzes the variation in an on-chip optical signal distribution system, determines the sources of variation involved and the degree to which they affect robustness of the system, and provides a comparison to a traditional H-tree electrical
signal distribution system. Variation sources do not inhibit the functionality of optical signaling, but measures must be taken to limit the impact of variation to ensure its robustness in the presence of technology scaling without compromising the characteristics which make it a potential alternative to electrical interconnect.
Bibliography


