The chip-scale modeling for CMP, presented by Tugbawa, can be problematic in both copper electroplating and subsequent CMP processes. Characterization and modeling of pattern-dependent issues and problems in both copper electroplating and subsequent CMP processes. The key underlying vehicle that enables characterization and modeling of pattern-dependent issues and problems in both copper electroplating and subsequent CMP processes. The chip-scale modeling for CMP, presented by Tugbawa, can be integrated with the work presented in this paper where the focus is on the development of a modeling methodology for electroplated surface topography.

The as-electroplated surface topography can be characterized by two height parameters: a feature scale step height (SH) and an array height (AH), as shown in Fig. 1 for a superfill (also known as bottom-up fill) electroplating process. SH is defined as the height associated with each copper line. If the copper sticks up due to the superfill effect, then the height is assigned a positive number; whereas, if the copper line recedes, as is common in conformal fill processes, then SH is assigned a negative number. AH is defined as the height difference between the top of the raised features in an array and the flat copper field region over wide oxide. Similar to the SH definition for positive and negative assignments, the AH is referenced to the field area which is defined to be at zero. Thus, when a bulge is present (as for fine line and fine space regions), the AH is positive, whereas, when the overall array region is recessed with respect to the field area, we have a negative AH. The magnitude of bulge or recess and SHs are dependent on feature sizes including both linewidth and space. For large features, conformal plating is observed, indicating that there is no impact on large features from the added chemistries used to achieve superfill. However, for fine arrays of lines, copper is filled above the field level nearby, and for large lines with fine spaces, a recess may be present in the copper surface topography. Also, it is possible to have copper sticking up above a trench when the trenches are narrow and spaces are large.

The remainder of this paper is organized into seven sections. The next section outlines the overall methodology for electroplating characterization and modeling, and the subsequent sections discuss in detail each part of the methodology. First, the test structure and mask design are described. Then, electroplating characterization is presented, followed by modeling of electroplated surface topography. We then describe layout parameter extraction and chip-scale simulation using the developed model. Finally, chip-scale plating prediction results are presented, and the conclusions are given.

Characterization and Modeling Methodology

An overall methodology for the development and application of a pattern-dependent electroplating model coupled to the characterization method is presented in Fig. 2 with an overall goal of chip-scale thickness simulations for any random layout. To characterize the as-plated copper topography variation for a particular electroplating process, a wafer patterned with a dedicated test mask is processed. Once a wafer is electroplated, we can measure SH, array bulge or recess, and field thickness to understand pattern-dependent behaviors in electroplated surface profiles. Based on key pattern dependencies and their trends, a semiempirical pattern-dependent model can be formulated that captures the key pattern effects as a function of underlying layout patterns. With characterization and model formulation, one can understand the fundamental limitations of these thickness variations for a specific process.

In addition to experimentally inducing and characterizing pattern-dependent thickness variations, we want to predict thickness variations across an entire chip by relating layout parameters such as pattern density and linewidth with calibrated model coefficients. Thus, a layout parameter extraction algorithm must be developed so that an extracted layout result can be efficiently used with the model in predicting chip-level variations. The calibrated model and extracted layout parameters are used with a chip-scale simulation procedure to predict chip-scale thickness variation for any arbitrary layout. Furthermore, the model-based simulation can be used to develop intelligent design rules for layout patterns to limit thickness variations. Detailed descriptions for each part of the methodology are presented in the subsequent sections.

Mask Description

The key underlying vehicle that enables characterization and modeling of copper interconnect pattern dependency is a test mask. The test mask described here is specifically designed to target layout pattern-dependent behavior and related studies for copper metallization including both electroplating and subsequent CMP planarization. This test mask has evolved from the original test mask version 0.0 through experimental studies and subsequent enhancements of mask designs.
To mimic interconnect, arrays of lines and spaces form the fundamental test structure for the study of pattern dependencies. Figure 3a shows a test structure that incorporates two regions or elements. The isolated line on the left gives the pattern effect due to an isolated line with minimal surrounding influence, and this is used to obtain isolated feature plating SH information. The array region gives information about array bulge or recess in electroplating, as well as feature SH within array lines. There is a separation of 300-500 μm between the isolated line and the associated array region, and this separation distance is large enough for the isolated line to be electroplated without array region influence. The entire array structure is relatively large (2000 × 2000 μm or larger) to maintain a uniform local pattern environment and is separated from neighboring structures (including the associated isolated line) by a substantial oxide spacing of 500 μm to decouple interactions among structures and to give a large field area to serve as measured surface profile reference points.

Using the basic line/array test pattern, the test mask consists of various combinations of linewidths and line spaces for covering a wide range of patterns to capture and identify key layout dependencies in the plating process. The mask is a single-level mask of die size 20 × 20 mm with a minimum geometry of 0.25 μm for linewidth and 0.25 μm for line space, and a maximum geometry of 500 μm lines. The layout of the test mask is shown in Fig. 3b, and the shaded areas (e.g., shaded lines) correspond to the test structures. The top two rows of structures are pitch structures, where the pitch is varied from 0.5 to 200 μm at a fixed pattern density of 50% (i.e., same linewidth and line space). Pitch is defined as the sum of linewidth and line space. The other main pattern structures are density structures, where the density is defined as the ratio of linewidth to pitch. The range of copper pattern density for these structures is from 10 to 90% for different pitch lines, where high copper density indicates wider linewidth and narrower space.

Surface Profile Characterization

This section presents the characterization of as-plated copper topography variation as a function of various underlying layout parameters such as linewidth and line space using the test mask as the vehicle. First, an experimental setup is described, followed by topography variation trends and characterization.

Experimental setup and measurement.—For this study, a short flow process is used where an 8 in. wafer is deposited with oxide, patterned, and etched with a nominal trench depth of 5500 Å. Then,
a tantalum-based barrier layer is deposited followed by copper seed deposition and electroplating using a Novellus tool. The nominal target thickness of 15,500 Å over wide field area (e.g., region without any trenches) is electroplated on the wafer surface.

Once the wafer is electroplated, we measure the relative surface heights for each of the patterns using a KLA-Tencor high-resolution profiler (HRP) as illustrated in Fig. 4. The figure shows two example scans for SH and AH which exhibit different electroplating characteristics: a superfill plating and a more conformal fill plating process. Positive and negative notation is used as described in the introduction.

**Characterization and trends.**—For our characterization, we want to quantitatively examine both the SH and AH as a function of various underlying layout parameters and identify key trends. First, the surface profile scans are examined to observe qualitative trends in electroplating. The wide range of pattern-induced surface topography variation is shown in Fig. 5. The surface profile scans are for pitch structures from 0.25 μm width and space to 100 μm width and space, as marked above each plot. Bulging of the array region can be seen for most of the structures in the top half of the figure, and a greater bulge is observed for narrower lines and spaces. However, the bulge decreases as the feature size increases, and the bulging effect becomes negligible for the arrays having 1 μm width and space. For the surface profile scans in the still larger pitch structures, the bulging effect is gone, and conformal deposition becomes more dominant with some recess seen for 2-10 μm array lines.

Furthermore, varying degrees of SH are observed: small features have practically no or very small SH, and large features show an SH saturated at approximately the designed trench depth. Similar bulging and conformal deposition characteristics are also present across different pattern structures (e.g., density structures), indicating that linewidth or space, rather than derived pattern factors of density and pitch, may be the dominant pattern factors influencing surface profile variation in electroplating.

These profiles provide qualitative insight into trends for various patterns. The SH and AH values, extracted from the surface profile scans, are then plotted as a function of underlying layout pattern factors. Figure 6 shows the SH as a function of the underlying line (copper trench) width. We can see from the top graph for the isolated lines that SH is positive for small isolated features, indicating a regime of superfill up to a linewidth of 1-2 μm. SH then becomes negative as linewidth increases further, indicating a more conformal fill. Note that after about 10 μm (marked by LW), the SH saturates at a trench depth of around 5500 Å. A similar behavior is observed for the array lines, where SH again depends strongly on linewidth. The different SH values for a particular linewidth are from structures with the same linewidth but different line spaces and indicate that there is also a line space dependence in the plated SH.

For the AH, we also find that the trends are best captured as functions of linewidth and space. Figure 7 shows the AH dependence on linewidth. The AH is positive for small features, indicating bulging of copper due to superfill behavior. The bulging effect is larger for small features and increases as the linewidth decreases. As the linewidth becomes larger (between 1 and 10 μm), the AH decreases and becomes negative, indicating array recess. Then, as the linewidth increases further, the AH saturates and reaches zero beyond a linewidth of 10 μm (marked by LW). [When AH vs. line space is plotted, a similar behavior is observed, where the AH is positive for small line spaces and then becomes negative before saturating to zero at around 10 μm (marked by LS).] The saturation to zero array height for large line spaces indicates that beyond 10 μm of line space, the region can be treated as field area.

Overall, small features (small linewidths and spaces) show a superfill effect, where the SH and AH are large and positive. In con-
large features show conformal deposition, where the electroplated profile resembles the underlying trenches and spaces. The saturation width \( (L_W) \) and space \( (L_S) \) for the step height are approximately 10 \( \mu m \), and the same value is also observed as the saturation point in the AH trends. The SH and AH data can alternatively be examined as a function of pattern pitch or density to determine if there is a clear relationship between SH and these pattern factors. However, no clear trends in terms of these factors are observed.

**Model Development and Calibration**

We have seen that there are trends in electroplating that depend on the underlying layout parameters of linewidth and space.\(^5\) The next step is to develop a model that captures the surface topography variation. We propose a multivariate response surface model that captures the surface topography variation for an electroplating process as a function of underlying layout parameters. A response surface model is appropriate in our case because our goal is to capture the surface topography variation in an effective manner and apply the model to any arbitrary layout across an entire chip for a chip-scale simulation.

**Semiempirical pattern-dependent model.**—We want the response surface model to be physically motivated and able to capture the observed plating behavior. In a previous study,\(^6\) physical mechanisms of electroplating\(^7\)-\(^16\) were examined to derive response surface model variables. It was found that plating should depend on both the linewidth and line space for basic plating mechanisms based on Faraday’s law of electrolysis. For the superfill behavior, \( 1/width \) has a direct influence on the deposition rate and thus on the final surface profile.

Thus, based on the physically motivated model parameters of width, space, \( 1/width \), \( 1/width \) and \( \text{width} \times \text{space} \) interactions, plus the second-order terms \( (W^2 \) and \( W^{-2} \)) to capture any higher-order effects, the significance of each model factor is determined across five different data sets. The following response model is most effective at capturing AH and SH variations

\[
AH = aW + bW^{-1} + cW^{-2} + dS + eS(WS) + \text{Const}_A \tag{1}
\]

\[
SH = aS + bS^{-1} + cS^{-2} + dW + eW(S) + \text{Const}_S \tag{2}
\]

where \( W \) is linewidth, \( S \) is line space, \( AH \) is array height, and \( SH \) is step height as defined earlier. As \( W \) becomes small, the superfill effect is dominant, and the \( 1/W \) and \( 1/W^2 \) terms become dominant. As \( W \) increases, conformal fill is dominant, and the \( 1/W \) and \( 1/W^2 \) terms become small and the \( W, S \), and \( W \times S \) terms become dominant to capture the conformal trend. A superfill electroplating process typically used for current copper metallization exhibits both superfill and conformal regimes depending on the feature size. Both regimes are captured in the model form instead of modeling for two regimes separately. This response surface model is tested over many sets of data from different plating recipes and different tools, and all fits are generally under 500 \( \AA \) of root-mean-square (rms) error.

**Model fit and model coefficient extraction.**—Statistical analysis and model fits are considered in this section to demonstrate model parameter significance and overall data fits. Table I summarizes the result of the regression for the SH data; the model coefficients as well as an rms error and the significance are indicated. The SH model fit is shown in Fig. 8 as a function of linewidth; the overall
trend is well captured with a model $R^2$ of 0.9793 and a fitting rms error of around $330 \text{ Å}$. Also, the significance test, $Pr (>|t|)$, indicates that the model coefficients are all highly significant (to greater than 99.99% confidence).

For the AH fit, the constant and $S (d_\lambda)$ terms are only marginally significant, and the $1/W (b_\lambda)$ term is not significant. Thus, in this particular case, coefficient $b_\lambda$ is set to zero, and the model is refitted to data using the simplified model form

$$AH = a_\lambda W + c_\lambda W^{-2} + d_\lambda S + e_\lambda (WS) + \text{Const}_\lambda \quad [3]$$

The obtained new set of model parameters, summarized in Table II, shows that the simplified model form is more significant and still captures the trend well. Our general model framework can be simplified in some cases depending on the electroplating process, and the model fit discovers this simplification as a natural part of the regression. The model fit vs. data is shown in Fig. 9 with the "better" simplified model. The fit for AH vs. linewidth captures both the superfill trends for small features and the conformal fill trends for large features. The rms error for the model fit is about $424 \text{ Å}$, and the $R^2$ value is 0.9546.

The model shows good correlation between the data and the fit for both step and array height, and captures both the superfill effect for fine features and conformal fill for large features. The use of the model and the extracted model coefficients enables us to perform chip-level simulations, which are the focus of the next section.

**Chip-Scale Simulation Procedure**

The chip-scale simulation of electroplated topography is done by computing a generalized “average” AH and SH for a grid cell, where the grid cells are equally divided small regions on a die. The procedure for obtaining relevant layout information and using this information to perform chip-scale simulation is explained in detail in the next two sections, respectively. First, an example is used to illustrate the calculation of the average or effective AH and SH for a given grid cell, which is the key enabler for efficient chip-scale simulation. In this work, we choose a grid discretization using 40...
$3 \times 40 \, \mu m$ cells. This is a trade-off between several considerations of sampling resolution, characteristic length scales in plating, and compatibility with the needs of subsequent CMP simulation.

**Basis of topography averaging for chip-scale simulation.**—An example cell is shown in Fig. 10, consisting of two regions with different copper linewidths and spaces. Region A occupies the left 24 $\mu m$ wide portion of the cell, and region B occupies the right 16 $\mu m$ portion of the 40 $\mu m$ wide grid cell. In the electroplated profile labeled Case 1 in the lower part of Fig. 10, region A has a plated $AH$ of $2000 \, \AA$ and an $SH$ of $3000 \, \AA$, and region B has an $AH$ of 0 $\AA$ and an $SH$ of $5000 \, \AA$. In the simplest approach, we might find an “average” $AH$ and $SH$ for this grid cell by computing the area-weighted averages as follows:

$$AH_{\text{avg}} = \frac{-2000 \times 24 \, \mu m + 0 \times 16 \, \mu m}{40 \, \mu m}$$

$$= -1200 \, \AA$$ [4]

Using a similar method, we can find a positive $AH_{\text{avg}}$ of 900 $\AA$ ($=1500 \times 24/40$) and $SH_{\text{avg}}$ of $-2000 \, \AA$ ($=-5000 \times 16/40$) for the alternative electroplated profile labeled Case 2, which has a pronounced array bulge for the region A.

However, this simple average must be generalized in an important way to account for positive and negative $SH$ values. A scenario where the effective $SH$ is calculated to be zero even from existing $SH$ topography helps to illustrate the problem. In a situation where half of the grid cell has a positive $SH$ of 3000 $\AA$ and the other half has a negative $SH$ of the same amount, the average $SH$ is computed to be zero. An $SH$ of zero suggests that the surface is flat or smooth, but this is not the case here. Thus, we generalize the “average” $SH$ calculation to the following:

$$SH_{\text{avg}} = \left( |SH_A| \times \text{area}_A + |SH_B| \times \text{area}_B \right) / \text{Total Area}$$ [6]

where we take the absolute $SH$ value of each region A and B, weight by the area occupied by each respective region, and divide by the total area.

**Layout parameter extraction.**—The next challenge is to extract meaningful information from the layout geometry data for each cell. Figure 11 shows an example grid cell for a random layout that contains a variety of feature sizes in both vertical or horizontal line orientations. We are interested in extracting the linewidth and line

![Step Height vs. Line Width](image1)

**Figure 6.** $SH$ vs. linewidth for isolated lines and array lines.

| $SH$ model coefficients | Extracted values | Standard error | $t$ value | $Pr (>|t|)$ |
|-------------------------|-----------------|----------------|-----------|------------|
| $a_S$                   | -663.18         | 108.05         | -6.14     | 0.0000     |
| $b_S$                   | -357.23         | 80.74          | -4.42     | 0.0001     |
| $c_S$                   | 60.45           | 10.50          | 5.76      | 0.0000     |
| $d_S$                   | 115.56          | 17.26          | 6.69      | 0.0000     |
| $e_S$                   | -69.11          | 9.16           | -7.54     | 0.0000     |
| Const$_S$               | 1075.22         | 245.02         | 4.39      | 0.0001     |

rms error = 327 $\AA$. $R^2 = 0.9793$. Overall significance: $P$ value = 0.

$$SH_{\text{avg}} = \left( -3000 \times 24 \, \mu m + (-5000 \times 16 \, \mu m) \right) / 40 \, \mu m$$

$$= -3800 \, \AA$$ [5]

**Table 1. $SH$ fit.**

![Step Height Fit vs. Line Width](image2)

**Figure 7.** $AH$ vs. linewidth.

**Figure 8.** $SH$ model fit vs. linewidth.
space information for each cell. Regardless of direction of lines, for consistency we require that the shorter dimension of the rectangle be taken as the linewidth \( W \) and the longer dimension be taken as the line length \( L \), as shown in Fig. 11. When the layout object is a polygon, the polygon is split into a set of rectangles, and the same rule applies in determining which dimension is \( W \) and which dimension is \( L \) for each rectangle. When a line occupies two neighboring grid cells, we still use the same definition of width and length, but use the full width and length of the layout object and not the object cut off at the grid box boundaries. Using this definition of linewidth and line length, layout parameter extraction is done for each cell, and eventually both SH and AH simulation are performed on a cell-by-cell basis.

In a typical layout, there are many lines of different widths within a cell. A simple approach might be to use the average linewidth and average line space (derived from the copper pattern density and average linewidth) to perform the electroplating simulation. However, the result would be a poor approximation, because the AH and SH values depend in a nonlinear fashion on the linewidths. In this work, we propose to use a binning approximation to the distribution of linewidths reported from the layout extractor, and then to use this information to further generalize the computation of “average” AH and SH within the cell.

In this method, the layout extractor gives a count of the number of lines having a linewidth in each bin of the linewidth distribution. We illustrate this using an example shown in Fig. 10 having a regular array of lines for simplification. Region A contains eight lines of width 1.5 \( \mu \)m and space 1.5 \( \mu \)m, and region B contains three lines of width 4 \( \mu \)m and space 2 \( \mu \)m. Thus, for this cell, the minimum width is 1.5 \( \mu \)m and the maximum width is 4 \( \mu \)m. The average width is \((8 \times 1.5 + 3 \times 4) / 11\), which is 2.182 \( \mu \)m. For our example, the total area occupied by copper is \((8 \times 1.5 \times 40 + 3 \times 4 \times 40)\), which is 960 \( \mu \)m\(^2\); and the total area of the grid cell is 40 \times 40, which is 1600 \( \mu \)m\(^2\). Thus the copper pattern density, defined as the

### Table II. AH new model form (without \( 1/w \) term) fit.

| AH model coefficients | Extracted values | Standard error | \( t \) value | \( P(>|t|) \) |
|-----------------------|-----------------|----------------|-------------|-----------|
| \( a_A \)            | -887.3203       | 108.4705       | -8.1803     | 0.0000    |
| \( b_A \)            | 0               | NA             | NA          | NA        |
| \( c_A \)            | 263.8060        | 29.4506        | 8.9576      | 0.0000    |
| \( d_A \)            | -128.2050       | 91.1012        | -1.4073     | 0.1755    |
| \( e_A \)            | 93.4935         | 13.5594        | 6.8951      | 0.0000    |
| \( \text{Const}_A \) | 717.0528        | 281.9886       | 2.5428      | 0.0199    |

rms error = 424 Å, \( R^2 = 0.9546 \). Overall significance: \( P \) value = 1.773 \times 10^{-12}.

![Figure 9. AH model fit vs. linewidth.](image)

![Figure 10. Example grid cell and cross-sectional view of plated profile.](image)

![Figure 11. Definition of linewidth and line length.](image)
The cutoff values of linewidth for each bin are chosen so that the nonlinear trends can be approximately linearized within each bin. The layout extractor reports the following layout information for each cell: X and Y location of cell center, minimum linewidth, average linewidth, maximum linewidth, linewidth bins, total count of lines, average line length, and copper pattern density. For the linewidth bins, eight lines are reported in bin 4, and three counts in bin 5 for our example. Note that the current layout tool is limited in only calculating information on the linewidth, but not on the line space. Thus, line space distributions are not explicitly reported.

**Modeling of chip-scale simulation for AH and SH.**—The extracted layout parameters are input to the semiaempirical plating model to perform the simulations for each grid cell in the chip. This section describes the procedure for performing a chip-scale simulation based on the binned extracted layout information. The key idea is to generalize the “average” SH and AH as a weighted average of plating heights across the binned layout information.

First, we assign one representative value for the linewidth for each bin by using the mean of the low and high cutoff values for that bin. For example, our second bin is from a linewidth of 0.35 to 0.5 μm, so 0.425 μm is used as the representative value of the width for that particular bin. One exception to this rule is the assigned width for bin 7, where the characteristic length, $L_w$, is used as the representative linewidth.

Because the current extractor tool is limited to calculating information on linewidth only, an average line space is derived from the layout extraction result given by using the definition of copper pattern density, $\rho_c$, for arrays of lines as indicated in Eq. 7

$$\rho_c = \frac{W}{W + S} \quad [7]$$

This can be rearranged to give line space S in terms of the available copper pattern density and width

$$S = \frac{W(1 - \rho_c)}{\rho_c} \quad [8]$$

where $S_i$ is the space for the ith bin derived from $p_c$ and $W_i$ is the assigned linewidth for the ith bin. Before the simulation can be performed, we need to derive the area occupied by the lines in each bin, as indicated in Eq. 9

$$A_i = W_i N_i \bar{L} \quad [9]$$

where $N_i$ is the number of lines in the ith bin, and $\bar{L}$ is the average line length in the grid cell.

Given this preparation, the AH and SH simulations can now be performed. First, the AH and SH values are calculated for each bin $i$ as described in Eq. 10 and 11

$$AH_i = a_A W_i + b_A W_i^{-1} + c_A W_i^{-2} + d_A S_i + e_A (W_i S_i) + \text{Const}_A \quad [10]$$

$$SH_i = a_S W_i + b_S W_i^{-1} + c_S W_i^{-2} + d_S S_i + e_S (W_i S_i) + \text{Const}_S \quad [11]$$

where $\lambda_A$ through $\lambda_e$ and $\lambda_s$ through $\lambda_e$ are the empirically extracted model coefficients for AH and SH, respectively. Once individual array and step heights are found for each bin, the generalized AH and SH are determined by an area-weighted average as follows

$$AH = \frac{0 \quad \text{Total count} = 0 \quad \text{or} \quad \rho_c < 0.01}{-H_o \quad \rho_c > 0.99} \sum_i (AH_i; A_i) \quad [12]$$

otherwise

$$SH = \frac{0 \quad \text{Total count} = 0 \quad \text{or} \quad \rho_c < 0.01}{0 \quad \rho_c > 0.99} \sum_i (SH_i; A_i) \quad [13]$$

otherwise

where the total area $A$ is the sum of each bin area $A_i$, or $A = \Sigma A_i$, as computed in Eq. 9. Some special cases must be considered. When the copper pattern density is near zero, or the total count is zero, there are no lines in that grid cell, and the cell represents a field region on the chip. Thus, AH is zero and SH is zero. Another boundary case is when the copper pattern density is close to 1 (100%). This indicates that the grid cell is nearly all trench fill, as if the grid region comes from a middle of a large line or pad on the chip which would be filled conformally. Thus, AH is set to $-H_o$, where $H_o$ (a positive number) is the initial trench depth, and SH is set to zero. The computation of AH and SH as expressed in Eq. 12 and 13 (including the special cases just discussed) is then repeated for all grid cells in the chip to yield a complete chip-scale simulation of the electroplated topography.

**Field thickness variation: Extraction and simulation.**—Up to this point, we have dealt with AH and SH variations, and have assumed that the nearby wide field regions without any patterned trenches are flat. However, experimental results indicate that there is systematic
nonnegligible field thickness variation. In this section, we describe an extension of the chip-scale simulation to incorporate this additional field thickness variation.

Measurements are taken using the Metapulse tool by Rudolph Technologies on field regions between array structures, marked by numbers indicated on the test mask, as seen in Fig. 13a. The measured data is shown in Fig. 13b, where the range of field thickness is about 1400 Å, and the average is 15,325 Å, which is close to the nominal target thickness of 15,500 Å.

For the measurement sites 1 through 7, the array regions next to each site increase in pitch, and for the measurements sites 8 through 14, the array regions next to each site decrease in pitch. The data indicates that there is an increase in field thickness if there are array regions nearby with large pitch values, and there is a decrease in field thickness if there are array regions nearby with smaller pitch values. Also, it is observed that measurement site 21, which is surrounded by a larger field region, has one of the largest field thicknesses. This observation of a systematic trend indicates that another longer length scale may be at work. The field thickness may depend on nearby structures in a region on the order of hundreds of micrometers, if not millimeters, around the field region of interest because the distance from a field measurement site to a nearby array region is around 0.5-1 mm.

The physical origins of this effect are not clear. However, here we seek again to generate a semiempirical model to capture the observed effect and leave physical investigation to future work. We propose an approach in which we frame the field thickness ($FT$) variation as a function of the underlying layout patterns, rather than as a function of nearby fill, as shown in Eq. 15.

$$FT(x, y) = f(\text{layout pattern}, P) \quad [15]$$

Here $P$ is a model parameter that specifies the size of the region that influences a particular point of interest.

To capture the field thickness variation, we find an average “surface area” computed over a region of size $P$ on the chip. This surface area parameter, or $SA$, tracks both linewidth and space simultaneously and is conceptually based on a total “exposed” surface area accounting for sidewalls as well as the tops and bottoms of features, as illustrated in Fig. 14. The surface area is defined as follows

$$SA_g = A_W + A_B + A_S = N \cdot \bar{L} \cdot 2H_o + G^2 \quad [16]$$

where $SA_g$ is the surface area for grid cell $g$, $A_W$ is the sidewall area, $A_B$ is the area of the bottom of the trench, $A_S$ is the area of spacing, $N$ is the total number of lines in the cell, $\bar{L}$ is the average line length, and $H_o$ is the patterned trench depth. Here $G$ is the grid size, in our case 40 μm.

Based on the surface area $SA_g$, we formulate the following relationship from Eq. 15 to capture the field thickness variation for each grid cell $g$
where \( a, C, \) and \( F \) are common model parameters for all of the grid cells. Here \( C \) is a constant surface area offset term, and \( F \) is a field thickness constant term. \( \overline{SA_g} \) is the average surface area computed over a distance \( P \). Thus, \( \overline{SA_g} \) is an averaged value of the underlying cell \( SA_g \) values, where the average is taken across a substantial number, \( (P/G)^2 \), of nearby cells. In determining the value of model parameters, \( \overline{SA_g} \) is computed for a range of values of \( P \) up to 10 mm, which is half the size of our die. Then, for each candidate \( P \) and resulting \( \overline{SA_g} \), the model is fit to the data to determine the fit error, and the optimal field thickness model parameters are selected for the case with lowest fit error. This long-range averaging computation of field thickness is similar to the “planarization length” averaging used in pattern density-based CMP models and produces a smoothly or slowly varying field thickness across the entire chip. The model parameter extraction result is summarized in Table IV and Fig. 15 and indicates that all model variables are significant with a good model fit.

Using the field thickness variation predicted by this model, instead of the nominal or uniform average for field thickness, the final copper thickness, \( TT_g \), can be found as the sum of the field thickness and the AH in each grid \( g \)

\[
TT_g = \alpha(\overline{SA_g} - C) + F
\]

Second, prediction results are shown to determine how well the fitted model applies to a different “random” layout.

**Chip-scale simulation calibration results.**—Figure 16 shows the result of the chip-scale simulation of AH and SH on the test mask (MIT mask version 1.2) that is used to calibrate the model. Qualitatively, the AH and SH maps resemble the structures on the test mask. For instance, the topmost left corner is a structure with the smallest feature size on this mask, and the AH simulation is the highest in that array region, as we have seen in the AH trend. When the simulation result is compared to the data used to calibrate the model, the rms errors of AH and SH are 440 and 420 Å, respectively. These values are slightly larger than the fitting rms errors of 430 and 330 Å for AH and SH models, respectively, in the underlying feature level models. The small increase in the error is due to the fact that we are now dealing with distribution and derived layout parameter values, rather than true values of linewidth and space in the layout. The closeness of the chip-scale values to the fit errors appears to confirm that the generalized averaging approach proposed in the section on the chip-scale simulation procedure is a good approximation.

**Chip-scale prediction and verification result for arbitrary layout.**—This section presents simulation results and the verification.
for predicting the surface topography for a different complex layout as described in the section on characterization and modeling methodology. For this verification of the chip-scale prediction, a patterned wafer containing both test structures and product-like regions is electroplated with the same process used to calibrate the model. After the wafer is electroplated, measurements of AH, SH, and copper field thickness are taken at about 60 locations in a representative die and compared to the prediction result from the chip-scale simulation.

Figure 17 shows the prediction result of the chip-scale simulation for the AH and the comparison to measurement data. The comparison shows that the rms error is about 870 Å; for a nominal copper thickness of 15,000 Å, this corresponds to about 5.8% error. We note that in some regions (sites 10 to 40), the model overpredicts the magnitude of AH. This is believed to be caused by nearby dummy fills around the measured region consisting of lines that span about 10-20 μm wide; the simulation accounts for these dummy fills in its 40 μm wide cell, whereas our measurement is done for the AH created by the lines excluding the nearby dummy fills. In other regions that are more product chip like (sites 40 to 55), the model predicts relatively little AH, while ±1000 Å is observed. This may be due to difficulties and errors in the measurement of AH where there are no clearly defined field areas to level profile surface traces.

The field thickness variation across the entire chip is shown in Fig. 19 with the comparison to data shown on the right of the figure. The field thickness model produces a good first-order prediction. The plot of field thickness vs. average surface area shows that the electroplated field copper is thinner in regions with higher average surface area of the layout patterns; these cause a greater bulging effect, and this bulged region reduces the field thickness nearby.

By adding the field thickness result to the AH, the total copper thickness is obtained, as shown in Fig. 20a. The prediction indicates

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**Figure 17.** Chip-scale prediction and verification: AH.

**Figure 18.** Chip-scale prediction and verification: SH.
that the thickness varies from 0.9 to almost 2 μm, which gives a range of more than 1 μm thickness difference across the chip. In addition to thickness and relative height predictions, the layout density and as-plated topography density are shown in Fig. 20b and c. Similar to the result for the test mask, there is a great difference between the layout density and the topography density. The topography density is an important input to the subsequent CMP process modeling, which relates removal rate to pattern density of raised features.

We have described the result of the chip-scale prediction for a complex layout and verified it with actual data. There is a good match between the prediction result and the measured data.

Conclusions

This paper has presented a methodology for chip-scale modeling of electroplated copper surface topography. A dedicated test mask, consisting of a wide range of patterns, is used as a vehicle to capture the key pattern dependencies. Based on the characterization, a semi-empirical response surface model is developed. Once the model is calibrated using experimental data for a particular plating process, it is applied to perform chip-scale simulation for surface topography variation. Chip-scale simulation is based on average topography on a 40 × 40 μm discretized grid through the concept of average AH and average SH.

Figure 19. Chip-scale prediction and verification: Field thickness.

Figure 20. Chip-scale prediction. (a) Final thickness, (b) layout density, and (c) topography density.
To perform the SH and AH simulations across an entire chip, layout parameters are extracted based on distributions of line sizes from the layout within this grid. Then, the chip-scale simulation procedure is carried out to obtain the surface topography variation for that chip; we demonstrate successful simulation for a complex layout different than that used to calibrate the plating model for prediction of chip-scale topography variations including the field region thickness variation across the chip. We have found a good match between the prediction result and measured data. This methodology provides the first known chip-scale prediction of electroplated topography.

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