Analysis of DRIE Uniformity
for
Microelectromechanical Systems

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Abstract

A quantitative model capturing pattern density effects in Deep Reactive Ion Etch (DRIE), which are important in MEMS, is presented. Our previous work has explored the causes of wafer-level variation and demonstrated die-to-die interactions resulting from pattern density and reactant species consumption. Several reports have focused on experimental evidence and modeling of feature level (aspect ratio) dependencies. This thesis contributes a computationally efficient and effective modeling approach which focuses on layout pattern density-induced nonuniformity in DRIE. This is a key component in an integrated model combining wafer-, die-, and feature-level DRIE dependencies to predict etch depth for an input layout and a characterized etch tool and process. The modeling approach proposed here is inspired by previous work in modeling of chemical mechanical polishing (CMP). Computationally, this involves the convolution of an etch “layout impulse response” function or filter with the layout information (or equivalently but more efficiently the multiplication of FFTs).

The proposed model is validated by using a mask layer from the MIT Microengine project as a demonstration layout. The model can be tuned to predict the etch behavior to an accuracy of 0.1% RMS normalized error. Furthermore, a feature level model, which considers the effects of sidewall loading on the depletion of reactants is presented. Finally, methods of synthesizing dummy features to improve across-die uniformity in a layout are explored; a by tiling bare areas of the wafer into “fill zones,” an improvement in intra-die uniformity is seen.

In summary, a semi-empirical modeling approach has been developed for predicting the layout dependent pattern density nonuniformities present in DRIE. The approach can be tuned to specific tools and processes, and is computationally efficient. The model can serve as the basis for layout optimization to improve DRIE uniformity.

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Chapter 1

Introduction and Motivation for Research

This chapter presents the motivation for studying variation in deep reactive ion etch due to pattern dependencies, and the need for accurate prediction and dummy fill insertion. After giving a description of the physical processes involved in DRIE, we discuss previous work in the field. This thesis attempts to capture DRIE variation through a pattern-density based model, and to improve across die variation through the simulation of dummy fill structures.

1.1 Motivation and Overview

Microelectromechanical systems (MEMS) have become increasingly prevalent in recent years. One of the most important technologies for these devices is Deep Reactive Ion Etching (DRIE). DRIE involves cycles of etching and polymer deposition, which can produce extremely high aspect ratio structures with smooth sidewalls. For this process to be viable in high-volume manufacturing, design rules and methods must be developed to produce more uniform etch behavior across a single wafer.

This thesis has several goals. The first is to develop a pattern-density based method for predicting etch variation. The next is the implementation of rule-based dummy fill into a MEMS layout. The presence of these structures will balance the local loading density of the mask, which should result in more uniform etching of the structures.

Chapter 2 will describe in detail variation on the wafer-, die-, and feature-level scales. Chapter 3 will describe the pattern density model and its validation using a layout from the MIT Microengine project. Chapter 4 describes our efforts to create an aspect ratio dependent etch (ARDE) model that considers the effect of sidewall loading, and thus
integrates with the pattern-density based etch model. Chapter 5 presents simulations and strategies regarding dummy fill for MEMS. Finally, Chapter 6 is an overall conclusion and discussion of future work.

1.2 A Case Study of DRIE Uniformity: The microbearing rig

Recently Miki et al. studied DRIE uniformity in a power-generating MEMS device [1]. The microbearing rig is one of several multi-wafer fusion-bonded, rotating power MEMS devices under the umbrella of the MIT Microengine project. Two elements of this device, the rotor and stator blades, are shown in Figure 1-1. Like the turbopump device that will be studied in Chapter 3, the rig features extruded blades (on the rotor) which are realized via DRIE. The rotor, which is designed to rotate at 2.4 million RPM, is prone to failure caused by variation in blade thickness. This variation in thickness causes instability in rotation as pictured in Figure 1-1: differences in blade thickness causes eccentricity, or a difference in the location of the center of mass and the geometric center. The eccentricity causes the rotor to wobble during rotation, and when it becomes greater than the bearing clearance, device failure results [1].

![Figure 1-1 – Image of rotor blade for microbearing rig device](image)

Figure 1-1 – Image of rotor blade for microbearing rig device [1].
Dies near the edge of the wafer were found to etch 10% deeper than center dies, as summarized in Figure 1-3. Wafer and die-level variation were decomposed through Fourier analysis. The first component was attributed to global variation since it was more prevalent in edge dies. Miki et al. concluded that the second harmonic represents local interaction of features. Global etch variation was minimized by optimizing the APC angle, and thus improving the wafer-level uniformity. While chip and feature-scale uniformity was identified, a strategy to model or reduce it was not proposed.
1.3 **Overview of DRIE**

Although it is most commonly associated with MEMS, the Bosch process was originally developed for IC processing (STI, trench capacitors, and other structures with high aspect ratios). Researchers sought a repeatable method of etching trenches with well-controlled dimensions. At the time, issues with sidewall profiles were causing significant problems in IC fabrication. Specifically, undercutting in trench profiles often created voids during subsequent deposition steps, and roughness on the trench bottom resulted in reduced dielectric integrity and the formation of defects during oxidation. The fact that most etching at the time was done in batch reactors introduced more problems. Examples include high nonuniformity, poor Si/photoresist selectivity, and machine downtime due to material deposition on chamber walls. All of these factors led to the development of the serial Bosch etching schemes used today [2].

![Figure 1-4 – Schematic of a modern DRIE system [3]](image)

Most modern DRIE systems have a setup somewhat similar to Figure 1-4. Generally, a single wafer sits in a cylindrical chamber and is exposed to gases from
above. The supporting structure has electrodes which provide a wafer back bias. Additionally, helium gas flows across the wafer backside to keep the temperature constant. The RF coils excite the etching gas into a plasma. The automated pressure control (APC) regulates the pressure in the chamber.

1.3.1 Physical and Chemical Processes in DRIE

Bosch etching involves two major mechanisms: ion-assisted dry chemical etching, and polymer deposition. The interplay of three physical processes is vital in realizing high aspect ratio structures. The first component is dry chemical etching. Usually a combination of an oxide layer and thick resist is used as a masking layer, which is necessary because of both the non-selectivity of the ion etch and the length of the process. The chemical etch process is isotropic and leaves a circularly shaped opening. This isotropic etch is the main cause of the sidewall “scalloping effect” shown in Figure 1-5 (d). The next component in the Bosch process is polymer deposition. A conformal layer is deposited across the wafer. Finally the last component consists of ions, which directionally etch surfaces perpendicular to ion paths, including the polymer on the wafer surface and the trench bottom. The ions originate in the plasma sheath, which is created by the RF coil. Specifically, the coil produces a time varying magnetic field, which in turn creates an azimuthal electric field, as shown in Figure 1-6 [3]. In typical practice, only dry chemical etching occurs simultaneously with ion-assisted etching; this etch cycle alternates with the polymer deposition step to achieve high aspect ratio etching. These two steps are partially overlapped to optimize the trench profile.

The previous description was purposely vague about the chemicals used because several different combinations are possible. Although SF$_6$ and C$_4$F$_8$ are the standard
gases, Table 1-1 gives information about alternative Bosch chemistries. However, this thesis will focus on a specific combination of SF₆/C₄F₈.

![Figure 1-5](image1.png)

Figure 1-5 - The steps of DRIE include (a) photoresist patterning, (b) isotropic etching, (c) polymer deposition, (d) ionic polymer removal and isotropic etching.

![Figure 1-6](image2.png)

Figure 1-6 - Illustration of the overlap between Bosch steps [4].

### Table 1-1 - Information about alternative DRIE chemistries [5].

<table>
<thead>
<tr>
<th>Etch chemistry</th>
<th>HBr/BCl₃</th>
<th>HBr/SiCl₄</th>
</tr>
</thead>
<tbody>
<tr>
<td>substrate temperature</td>
<td>5°C</td>
<td>5°C</td>
</tr>
<tr>
<td>Masking layer</td>
<td>oxide</td>
<td>Oxide</td>
</tr>
<tr>
<td>etching gas</td>
<td>BCl₃</td>
<td>SiCl₄</td>
</tr>
<tr>
<td>Polymer deposition layer</td>
<td>HBr</td>
<td>HBr</td>
</tr>
<tr>
<td>Si etch rate</td>
<td>17000 angstroms/min</td>
<td>2 µm/min</td>
</tr>
<tr>
<td>Mask etch rate</td>
<td>280 angstroms/min</td>
<td>N/A</td>
</tr>
<tr>
<td>Si:SiO₂ selectivity</td>
<td>60 to 1</td>
<td>15 to 1</td>
</tr>
<tr>
<td>Si etch rate nonuniformity</td>
<td>2%</td>
<td>1%</td>
</tr>
</tbody>
</table>
The favored SF$_6$/C$_4$F$_8$ scheme performs substantially better than the alternative chemistries. Specifically, etch rates of up to 4µm/min can be achieved. The oxide selectivity can be 200:1, while the resist selectivity can reach 100:1. The following chemical equations describe the chemical process is involved in DRIE:

\[
SF_6 + e^- \rightarrow S_x F_y + S_x F_y + F^* + e^- \quad \text{(1.1)}
\]

\[
Si + nF^* \rightarrow SiF_n \quad \text{(1.2)}
\]

\[
C_4F_8 + e^- \rightarrow CF_x + CF_x^* + F^* + e^- \quad \text{(1.3)}
\]

\[
CF_x^* \rightarrow nCF_2 \quad \text{(1.4)}
\]

\[
nCF_2 + F^* \rightarrow CF_x^* \rightarrow CF_2 \quad \text{(1.5)}
\]

The first equation represents the dissociation of SF$_6$ into neutral fluorine radicals and ions. The fluorine radicals reach the wafer by diffusion, and are responsible for removing silicon. The S$_x$F$_y$ ions are accelerated by the plasma sheath, and remove the polymer film at the trench bottom. Equation 1.3 models the ionization of the fluorocarbon polymer, while Equation 1.4 shows the conversion of CF$_x$ to CF$_2$, which makes up the inhibiting layer. In a manner consistent with Equation 1.5, the remaining polymer film that was not removed by the ions is removed by the fluorine radicals.

1.4 Previous Work

1.4.1 DRIE

Much of the previous work involving DRIE (and plasma etch in general) has focused on basic physical understanding of the process. In a classic study of plasma etch, Gottscho et al. developed ion-synergism theory and created a useful vocabulary to describe the different causes of nonuniformity [7]. Coburn and Winters developed a
molecular transmission-based model which is useful in predicting aspect-ratio dependencies. More recently, Yeom et al. have explored the relation between pattern density and aspect ratio dependencies. The proposed theories will be discussed in detail in Chapter 2.

Other researchers have focused on process optimization and tool characterization. Ayon et al. were able to optimize etch behavior as a function of eight different process variables: SF$_6$ flow rate, SF$_6$ active time, etch overlap, electrode power during etch, C$_4$F$_8$ flow rate, C$_4$F$_8$ active time, electrode power during passivation, and APC angle.

![Figure 1-7 – Physical causes of variation in DRIE.](image)

We have determined several candidates for the physical causes of variation in DRIE, which are summarized in Figure 1-7. They include nonuniform distributions of fluorine radicals, ions, and waste products (SF$_4$). Additionally, non-uniform cooling across the wafer may also cause differences in etch rate. This thesis focuses on DRIE prediction with the assumption that gradients in fluorine distribution are the primary source of variation.

### 1.4.2 Dummy Fill

Work regarding dummy fill has mainly focused on chemical-mechanical planarization (CMP). Although some of the issues involved with CMP fill are moot in the
case of etch (capacitance, grounding, etc), the insertion strategies explored are still relevant. Rule and model based methods have been explored extensively, and dummy fill is a common feature in commercial integrated circuit manufacturing. The available fill strategies and how they apply to MEMS and DRIE will be revisited in Chapter 4.

1.5 Summary

As MEMS become a mature technology, layout optimization and other manufacturing concerns must be addressed. The goal of this thesis is to develop a model to capture pattern density based variation in DRIE. Additionally, dummy fill strategies will be explored as a variation reduction tool. The following chapters present the development and validation of the model.
Chapter 2

Theory of Deep Reactive Ion Etching

This chapter discusses the physical causes of variation on the wafer, die, and feature scales. The chapter begins with a discussion of terms commonly used in the literature to describe plasma etch variation. Next, the analytical models proposed for DRIE will be described. Finally, the application of the previous work to our formulation of wafer-, die-, and feature-level effects will be explored.

2.1 Vocabulary

Nonuniformities in plasma etch processes have been studied in one way or another continuously over the past 30 years. As a result, terminology has emerged for describing these variations. Specifically, microloading, Reactive Ion Etch (RIE) lag, ion shadowing, and neutral shadowing merit discussion. Other phenomena, such as micromasking and footing, have been described extensively in the literature, but these deviations from ideality within a single feature are not relevant to our focus on uniformity.

2.1.1 Microloading

Microloading is the relationship between local etch rate and pattern density. Features in high pattern density areas of a layout experience more competition for reactants, leading to a gradient in reactant flux, and to a slower etch rate. This effect is similar to the macroloading (dependence of reaction rate on etching surface area) effect originally explored by Mogab [6]. Although Mogab developed his theory which batch processing in mind, it is also applicable to the serial etching of wafers [7]. Specifically, an inverse
relationship exists between etch rate and the etchable area of silicon available, as shown in Figure 2-1.

![Figure 2-1 - Plot describing relationship between etch rate and 'loaded' area on wafer [8].](image)

Since microloading is so dependent on pattern density, it only makes sense to consider this effect when multiple features are present on a wafer.

2.1.2 RIE Lag

RIE Lag refers to the dependency of a feature’s etch rate on the aspect ratio (depth/width). Since the aspect ratio changes with depth, the etch rate evolves over time. Unlike the microloading effect, RIE lag is internal to a single feature. Two causes of RIE lag are ion and neutral shadowing; they will be discussed further in subsequent sections. In what is called ‘ordinary’ RIE lag, the etch rate decreases with increasing aspect ratio. Coburn and Winters suggest that the decrease is due to the diminishing probability of reactants reaching the trench bottom [9]. However, cases of etch rate increasing with aspect ratio have also been observed [10]. This phenomenon is called ‘reverse’ RIE lag.
2.1.3 Ion and Neutral Shadowing

Ion and neutral shadowing can be understood through simple geometric analysis. Consider the cross-section of feature, similar to one in Figure 2-2. As the trench etches deeper over time, the angular spread of the ions and neutrals that can reach the bottom becomes lower and lower. As a result the etch rate decreases. The ions have a smaller angular spread because they have been accelerated through the plasma sheath potential.

![Figure 2-2 - Illustration of shadowing effect [10].](image)

2.2 Analytical Models

The following section will briefly describe two of the more common physical models for plasma etch processes.

2.2.1 Ion Synergism Model

Ion synergism theory seeks to describe etch rate as a function ion, neutral flux, and surface coverage (i.e. inverse of pattern density). The etch rate in terms of ion flux is given by
\[ R = k \theta E_i J_i \]  

where \( k \) is the volume of silicon removed per unit of ion energy, \( \theta \) represents the masked area of the surface, and \( E_i \) (eV) and \( J_i \) (cm\(^{-2}\)s\(^{-1}\)) represent average ion energy and flux, respectively. The dependence of etch rate on neutral flux is defined as

\[ R = \nu S_o (1 - \theta) J_n \]  

where \( \nu \) is volume of silicon removed per reacting molecule, \( S_o \) is the reaction probability for the bare surface, and \( J_n \) is the neutral flux. By combining these two relationships and eliminating the \( \theta \) dependence, the following expression is obtained

\[ R = \frac{kE_i J_i}{1 + \frac{kE_i J_i}{\nu S_o J_n}} \]  

This model is useful in that it describes etch rate in terms of both ion and neutral flux [7]. Additionally, there is an indirect dependence of pattern density \((1 - \theta)\). However, ion-synergism does not account for how the etch rate would change with increasing aspect ratios.

2.2.2 Coburn-Winters Model

A closed form expression for the etch rate can be found by using conservation of gas flow [9]. The expression in Equation 2.4 describes the different reactant fluxes entering and exiting a feature

\[ \nu_i - (1 - K)\nu_i - K(1 - S)\nu_b = S\nu_b \]  

where \( \nu_i \) represents the flux entering the feature, \((1 - K)\nu_i \) represents radicals which are reflected out of the feature without reaching the bottom, \( K(1 - S)\nu_b \) represents radicals which reach the bottom of the feature but do not react with the Si surface, and finally the \( S\nu_b \) term describes the remaining radicals which react with the trench bottom. The terms
$v_t$ and $v_b$ are the fluxes at the top and bottom of the feature respectively. $S$ represents the reaction probability of silicon; this quantity is sometimes referred to as the “sticking coefficient.”

Figure 2-3 – Diagram illustrating fluxes entering and exiting a feature.

Figure 2-4 – Reaction probability $K$ as a function of aspect ratio [11].
In Equation 2.4, $K$ is the molecular transmission probability, or likelihood that an incident molecule will reach the trench bottom by diffusion. $K$ is dependent on aspect ratio, and has been empirically tabulated in the literature [11]. The normalized etch rate can be thought of the ratio of fluxes $v_b$ and $v_t$, or

$$\frac{R}{R_o} = \frac{v_b}{v_t} = \frac{K}{K + S - KS}$$

(2.5)

$R_o$ is the etch rate as the aspect ratio approaches zero. One shortcoming of the model is that it assumes that all etching occurs via diffusion of neutrals. Furthermore it does not taking into account reaction of neutrals with the sidewalls. Our attempts to characterize our tool/process with respect to this model will be addressed in Chapter 4.

In our work we choose to describe DRIE variation on the wafer-, die-, and feature-level scales. The following section will connect the physical effects and models described above to our terminology.

### 2.3 Wafer-Level Variation

Global variation spans the entire wafer, and is related to ion and neutral transport in the chamber. Sun et al. make several observations about global loading which link it to ion-synergism theory [8]. For low pattern densities ion transport is the dominant factor in determining uniformity since neutrals are abundant everywhere. As a result, layouts with low loading (<10%) generally exhibit a “hot spot” with a higher than average etch rate. As the pattern density increases, the behavior is governed by neutral transport since the neutrals become depleted in the chamber, resulting in a “cold spot.” Examples of spatial etch maps with these characteristics are shown in Figure 2-5.
Figure 2-5 – Left: Global etch map for 0.06% loading, which features a “hot spot” at the middle left part of the wafer. Right: Wafer-level etch map for 17.6% loading, featuring a “cold spot” at the upper right region of the wafer.

2.4 Die-Level Variation

We define die-level variation as a local dependence of etch rate on pattern density. Qualitatively, die or regions on a die that are surrounded by highly loaded areas will etch more slowly, since they encounter more competition for reactants. This phenomenon is analogous to the ‘microloading effect’ described earlier.

2.5 Feature-Level Variation

Feature-level variation refers to changes in etch rate due to increasing aspect ratio. The Coburn-Winters model, despite its shortcomings, is the most apt to describe this effect. Describing aspect-ratio dependencies in terms of pattern density is a crucial step along the path to obtaining an analytical expression for depth as a function of time (as is possible in CMP).
2.6 Summary

This chapter reviewed the relevant terminology and models used to describe plasma etch, and discussed each of them in terms of wafer-, die-, and feature-level scales which have been designated for our pattern density based prediction model.
Chapter 3

A Pattern Density Based Etch Prediction Model

A quantitative model capturing Deep Reactive Ion Etch (DRIE) pattern density effects is presented [12]. Previous work has explored the causes of wafer-level variation and demonstrated die-level interactions resulting from pattern density and reactant species consumption [8]. Several reports have focused on experimental evidence and modeling of feature-level (aspect ratio) dependencies [13]. In contrast, in this chapter we contribute a computationally efficient and effective modeling approach that focuses on layout pattern density-induced nonuniformity in DRIE. A micro-scale engine turbopump layout is used to demonstrate the model, and a comparison between the model and experimental data is presented for all five dies in the layout. Finally, limitations in the current model and directions for future work are summarized.

3.1 Description of Model

In this chapter, we focus on a methodology for modeling pattern-density based variation in DRIE. By pattern density, we mean the area fraction of exposed surface on the wafer (that portion not blocked by an etch mask), and thus we are concerned with design or layout-specific variation in etch depth or rate due to pattern density variations across the chip and wafer. Our pattern density model convolves an etch “impulse response” with a local pattern density map for any given device layout, in order to predict die-level etch perturbations for that design. The layout for the full wafer (typically with several die) is analyzed, so that pattern-density based interactions between die are captured, as well as within-die pattern density perturbations. In addition, wafer level
nonuniformities based on an empirically derived model are applied, resulting in predicted etch maps for each die across the wafer.

**Figure 3-1** – Framework for pattern dependent modeling in DRIE. The solid lines show components included in the present model.

### 3.2 Die-Level Model

The physical rationale behind the pattern density model is described next, followed by model derivation and implementation.

#### 3.2.1 Physical Motivation for Pattern Density Effects

As discussed in Chapter 1, the Bosch process involves two major mechanisms: ion-assisted dry chemical etching, and the deposition of a polymer inhibiting layer. During the etch cycle, we assume that the ion-assisted etch rate will be affected by the concentration of the reactant species. That is to say, we assume key reactions are:
Equation 3.1 represents the dissociation of SF$_6$ into neutral fluorine radicals and ions. The fluorine radicals reach the wafer by diffusion, and are responsible for removing silicon. We assume that localized concentration gradients of fluorine radicals create spatial variations in etch rate. Pattern density dependencies thus result from the localized consumption of reactants on different regions of the wafer. We find that these depressions in concentration can occur on relatively long length scales, i.e., across several millimeters, and thus result in interaction between multiple die on a wafer. Qualitatively, die that are surrounded by highly loaded areas will etch more slowly, since they encounter more competition for reactants.

3.2.2 Pattern Density Model Development

Die-level interactions are empirically modeled through the use of an “etch impulse response.” This idea is analogous to a filter-based inter-layer dielectric (ILD) thickness prediction scheme for CMP proposed by Ouma et al. [14]. If $f(x,y)$ represents the spatial response to an impulse of pattern density, and $d(x,y)$ is a function describing the local spatial pattern density of a layout, then the die-level variation $z(x,y)$ is given by a convolution operation:

$$z(x,y) = f(x,y) \otimes d(x,y)$$  \hspace{1cm} (3.3)

In our current model, the impulse response is based on the diffusion equation solution for a spherical coordinate system with an inverse distance ($1/r$) dependence. An expression for the filter function is obtained for the reduction $C$ of reactant concentration at a radius $r$ from an arbitrary point on the wafer surface. Equation 3.4 represents...
diffusion of the species \( C \), with surface area limited to a half sphere. By rearranging terms and integrating we can obtain an expression for the concentration (Eq. 3.5). In this equation, there are two important parameters: the reaction rate \( k \) and the diffusion coefficient \( D \), which represent the consumption rate of silicon and transport rate of etchant to the wafer surface.

\[
2\pi r^2 D \frac{\partial C}{\partial r} = k
\]  
\[C = -\frac{k}{D} \frac{1}{2\pi r}\]

Based on Eq. 3.5, we have the (negative) impact on background reactant concentration as a function of distance away from each area of exposed silicon. This impulse response thus forms a filter, as given by Eq. 3.6 below and illustrated in Figure 3-2, that we can convolve with a representation of the open area (local pattern density) across the wafer. We allow for an empirical constant \( \alpha \) in order to scale the filter with respect to wafer-level effects.
A three-dimensional spatial representation for \( f \) is given in Figure 3-4. The derivation given above makes some assumptions about the geometry of the situation; it assumes a spherical symmetry exists. A more exact form might consider the boundaries of the chamber and the entrance point of the gas (not directly above the wafer), among other factors. While equation 3.6 gives a \( 1/r \) spatial dependence and a magnitude scaling parameter (the aggregate of \( k, D, \alpha \), and constants), other spatial forms may also be appropriate. For example, solution of the diffusion equation with a cylindrical dependence gives rise to a \( \ln(r) \) dependence. An alternative approach is to empirically fit the spatial dependence, e.g., to \( a/(c+r)^b \), allowing constants \( a, b, \) and \( c \) to be determined empirically.

### 3.2.3 Pattern Density Model Implementation

In our implementation of the etch variation model (as summarized in Figure 3-1), the pattern density model consists of the information related to the filter function. Specifically, the pattern density model consists of the filter function structure (\( 1/r \) in this case), and an aggregate scaling parameter which is fit using characterization data for a fixed etch recipe. An AutoCAD layout for the design of interest is processed through a layout density extraction tool (provided courtesy of Praesagus, Inc.). The local layout pattern density map is convolved with the filter function to produce the pattern density perturbation to the etch rate or depth. Increased computational efficiency may be achieved by using an FFT approach rather than direct convolution. We assume that wafer-, die-, and feature-level etch perturbations are additive: pattern density based
variation is added to a wafer-level uniformity prediction to produce an etch variation map for the entire wafer.

A set of test masks was designed to fit the pattern density model for a specific recipe. The masks, such as those pictured in Figure 3-3, have a small region (or a pair of regions) on the wafer consisting of concentric circles with pattern densities varying from 10 to 90%. Etch experiments are performed and etch depths measured at a variety of distances from the patterned regions. These give the spatial extent and magnitude of pattern density-induced etch perturbation to fit the model. The filter parameters were extracted on a 1 mm x 1 mm size grid; additional amplitude scaling of the filter may be necessary when applied to a layout having a smaller discretization.

Figure 3-3 – A mask featuring concentric circles with varying pattern density is used to obtain the etch impulse response. The small circles in a regular grid are open areas where the etch rate is measured.
Figure 3-4 – Three-dimensional image of filter impulse response \( f(x,y) \).

The experiments were carried out in an Inductively Coupled Plasma (ICP) etcher manufactured by Surface Technology Systems of Newport, UK. A listing of process parameters for the etch is given in Table 3-1.

### 3.3 Feature-Level Model

Feature-level effects include variations due to differing aspect ratios (depth to width) in individual etch features. It is thought that these variations are related to the probability of reactant transmission to the bottom of the feature, as described by Coburn and Winters [5]. Recent efforts by Yeom et al. to separate effects suggest a connection between pattern density and feature level uniformity [13]. The model does not presently include feature-level effects; addition of an existing or new feature-scale model must be done with care to be consistent with the pattern density model. Our ongoing work towards integrating feature-level dependencies is further explored in Chapter 4.
3.4 Wafer-Level Model

Wafer-level variation spans the entire wafer, and is related to ion and neutral transport in the plasma, as well as asymmetries in the geometry of the chamber [8]. As discussed in Chapter 2, for low loading densities ion transport is believed to be the dominant factor in determining uniformity. As a result, layouts with low loading (<10%) generally exhibit a “hot spot” with a higher than average etch rate. As the etch rate increases, the behavior is governed by neutral transport, resulting in a “cold spot.” For the etch variation model in this work, we use an empirical characterization of the wafer-level variation for a given recipe. A separate set of test masks with uniformly spaced measurement locations is used.

Figure 3-5 – Masks used to obtain wafer-level maps, for 4.4% (left) and 17.6% (right) loadings. Data from the points in red were used in creating the maps. The 4.4% map featured 2 mm diameter circles separated by 8 mm. The 17.6% map has 2 mm circles with a spacing of 4 mm.

Each mask has a different uniform pattern density, and thus the wafer-level uniformity map corresponding to different global loadings can be empirically captured. Examples of two of the designs used are given in Figure 3-5.

Figure 3-6 shows a normalized (to highest etch rate location) wafer-level spatial etch map corresponding to 4.4% global loading. In some etch applications (including the turbopump example shown later), the wafer is rotated multiple times during the total etch.
The wafer level model thus averages the spatial uniformity map through equivalent rotations.

![Normalized Wafer-Level Etch Map (4.4% loading)](image)

**Figure 3-6 – Normalized wafer-level etch map for 4.4% loading**

### 3.5 Model Application

While DRIE has been successful in a research environment, issues with uniformity remain a challenge for use in high volume MEMS manufacturing. An example of such a barrier can be found in the fabrication of microscale rotating power devices in silicon. These devices consist of bulk-micromachined layers bonded together, and rely heavily on DRIE. As described in the microbearing rig study in Chapter 1, etch nonuniformity can create variation in feature height, which may lead to imbalance in rotation and device failure [1]. The etch depth variation possible in a single device, based on WYKO measurement, is shown in Figure 3-9. For demonstration of the model we focus on the turbopump, which is very similar in construction to the microbearing rig discussed in Chapter 1. The individual turbopump is replicated multiple times on the wafer, resulting in a local density map as shown in Figure 3-7.
The extraction shown in Figure 3-7 (upper) is performed on a 100 µm by 100 µm grid. The red areas represent an open etch area, while the blue areas represent a masked area. The local density map is convolved with the impulse response to obtain the percentage etch rate variation due to pattern density. The result is added to the normalized global etch map corresponding to the layout (4.4% loading in the case). Rotation of the wafer during fabrication is simulated by rotating the wafer-level etch map and re-normalizing the result.
Table 3-1 – Process parameters for the turbopump etch

<table>
<thead>
<tr>
<th></th>
<th>Flow rate</th>
<th>Platen power</th>
<th>Coil power</th>
<th>APC</th>
<th>Pressure Trip</th>
</tr>
</thead>
<tbody>
<tr>
<td>SF₆</td>
<td>105 sccm</td>
<td>100 W</td>
<td>750 W</td>
<td>75°</td>
<td>94.0 mT</td>
</tr>
<tr>
<td>C₄F₈</td>
<td>40 sccm</td>
<td>60 W</td>
<td>600 W</td>
<td>75°</td>
<td>94.0 mT</td>
</tr>
</tbody>
</table>

The etch variation map was compared to a wafer etched for 90 minutes with a layout based on the extraction given in Fig. 4. The chamber parameters are identical to those used to obtain the filter coefficients. The wafer was rotated 90° four times to control the effects of wafer-level variation. Figure 3-8 through Figure 3-17 feature close-ups of the simulated pattern density variation and experimental data for each die. However, it should be noted that model was calibrated to points at a 2.2 mm radius from the center of the die rather than the entire die. Thus the die-level comparisons yield varying degrees of accuracy. For the upper left die in the layout, the predicted and measured across-die variations are relatively similar. The same can be said of the lower left die. The experimental data from the upper and lower dies diverges significantly from the model. Judging from the extremely high range of etch depths within these dies, issues with the measuring tool may be partially responsible. Table 3-2 summarizes simulated and experimental across-die variation for each die. Predictions for the turbopump mask, based on filter coefficients tuned using the characterization mask, are within 1% root-mean-square (RMS) error.
Figure 3-8 – Predicted across-die variation for upper left die (7.2%). The color scale represents normalized etch rate.

Figure 3-9 – Measured across-die variation for upper left die (6.8%). The color scale represents depth in microns.
Figure 3-10 – Measured across-die variation for upper right die (6.9%). The color scale represents normalized etch rate.

Figure 3-11 – Measured across-die variation for upper right die (9.2%). The color scale represents depth in microns.
Figure 3-12 – Simulated across die variation for the middle die (7.09%). The color scale represents normalized etch rate.

Figure 3-13 – Measured across die variation for center die. This die has the least variation in depth due to the presence of balanced loading on all sides. The color scale represents depth in microns.
Figure 3-14 – Simulated across die variation for lower left die. The color scale represents normalized etch rate.

Figure 3-15 – Experimental etch data for the lower left die. The color scale is depth in microns.
Figure 3-16 – Simulated etch variation for lower right die. The color scale represents normalized etch rate.

Figure 3-17 – Experimental etch data for lower right die. The color scale represents etched depth in microns.

As a further test, etch rate variations are also considered on a scale internal to a single die. In order to measure intra-die variation, depth measurements were taken at a 2.2 mm radius from the center of each die. Taking measurements at a constant radius minimizes
feature-level effects, since the feature opening will be similar along the circumference.

The numbering scheme for these positions is shown in Figure 3-18.

![Figure 3-18 – Measurement scheme for subsequent figures. The measurements were taken at a 2.2 mm radius for the die center.](image)

The pattern density model is able to capture the subtle spatial pattern of etch nonuniformity within this ring, as seen in Figure 3-19 through Figure 3-23, which show predictions and experimental measurements for the each of the five dies in the layout. The trends in the figure can be understood qualitatively: positions nearest to the center of the wafer layout have a higher pattern density, and experience a slower etch rate. The empirical scaling coefficient $\alpha$ is tuned to the turbopump data; without tuning, the correct spatial trends are captured but our 1% error results in offsets in the trends of Fig. 8. The filter magnitude tuning appears necessary to overcome model limitations. An $\alpha$ value of 2.34 was found to fit the data. The data was normalized by subtracting the max value from each point in the series, and then dividing by that value.
Figure 3-19 – Comparison between simulated and experimental etch rates for the upper left die. The model data is represented by squares; experimental data is in diamonds.

Figure 3-20 – Comparison between simulated and experimental etch rates for upper right die. The model data is represented by squares; experimental data is in diamonds.
Figure 3-21 - Comparison between simulated and experimental etch rates for the center die. The model data is represented by squares; experimental data is in diamonds.

Figure 3-22 – Comparison between simulated and experimental etch rates for the lower left die. The model data is represented by squares; experimental data is in diamonds.
Figure 3-23 – Comparison between experimental and simulated ER data for the lower right die. The model data is represented by squares; experimental data is in diamonds.

The tuning parameter allows intra-die variation to be accurately modeled. It should be noted that it is most difficult to model intra-die nonuniformity for the center die (see Figure 3-21) because it has the smallest range of etch rate variation. Table 3-2 summarizes the results from the turbopump demonstration.

<table>
<thead>
<tr>
<th></th>
<th>Die 1 (upper left)</th>
<th>Die 2 (upper right)</th>
<th>Die 3 (center)</th>
<th>Die 4 (lower left)</th>
<th>Die 5 (lower right)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Across die variation (predicted)</td>
<td>7.02%</td>
<td>6.90%</td>
<td>7.09%</td>
<td>6.97%</td>
<td>7.03%</td>
</tr>
<tr>
<td>Across die variation (actual)</td>
<td>6.80%</td>
<td>9.20%</td>
<td>3.90%</td>
<td>6.40%</td>
<td>8.50%</td>
</tr>
<tr>
<td>RMS Error</td>
<td>0.09%</td>
<td>0.08%</td>
<td>0.11%</td>
<td>0.03%</td>
<td>0.08%</td>
</tr>
</tbody>
</table>
3.5.1 Limitations and Future Work

A pattern density based model has been presented for spatial mapping of layout dependent effects in DRIE. The model is able to capture the large across-die variations (6-7%) existing in DRIE applications, such as the turbopump. The model can also capture subtle within-die effects, with additional tuning to achieve 0.1% accuracy. The pattern density model can serve as the basis for layout optimization (as will be discussed in Chapter 5) to improve DRIE uniformity.

Several limitations and possibilities for future improvements can be noted. First, alternative functional forms for the pattern density filter function (e.g. \(1/r^b\)) may be considered, or may apply in different etch circumstances. Second, feature-level or aspect-ratio dependent effects have not been included. Work is needed to understand how pattern density effects evolve over time as feature aspect ratios change. Third, the wafer-level model can be improved to predict wafer uniformity across varying global etch loadings by way of an improved physical model. Finally, alternative ways of combining these three components (e.g. in a multiplicative rather than additive manner) can be considered to account for wafer-, die-, and feature-level interactions.

3.6 Summary

This chapter has presented a methodology for modeling wafer-, die-, and feature-level variation. After presenting the model, verification of the model is accomplished using the turbopump mask as a demonstration layout.
Chapter 4

A Sidewall-Loading Model for Aspect Ratio Dependent Etching (ARDE)

This chapter will present a model for aspect-ratio dependent etch which accounts for sidewall loading. After describing the model and how the empirical parameters are fit to it, a comparison with other ARDE models (i.e., Coburn-Winters) will be made.

4.1 Sidewall Loading in ARDE

The Coburn-Winters model relies on the principle of Knudsen transport, meaning that each reactant molecule reflects off a feature’s sidewalls and can only react with the bottom of a feature. However, we can see from the chemical equation 1.5 in Chapter 1 that some fluorine radicals do interact with the polymer on the sidewalls.

Figure 4-1 – Illustration of molecular behavior with Knudsen transport (left trench) and the Sidewall Loading Model (right trench).

Figure 4-1 illustrates how Knudsen transport-based models impose more constraints on molecular behavior. In the left trench, an incident fluorine radical can either reach the trench bottom and react with the surface, or bounce off the sidewalls (and bottom) and be
reflected out. In contrast, a sidewall loading model allows radicals to react with the bottom, react with the sidewalls, or be reflected out of the trench.

Recent work by Yeom et al. suggests that Knudsen-transport based models are only valid for a limited range of aspect ratios [13]. For extremely low aspect ratios (i.e. $0 < \alpha < 1$) a nearly constant etch rate can be expected. Additionally, features with aspect ratios beyond a certain upper threshold will experience a precipitous drop off in etch rate. Figure 4-2 shows the approximate locations of these critical aspect ratios.

![Figure 4-2](image.png)

**Figure 4-2 – Illustration of three regimes of ARDE. The Knudsen transport regime is defined as (1<AR<25) [13].**

### 4.2 Model Development

When developing the sidewall loading model, we first consider what inputs and outputs are necessary. The model should be able to take pattern density, current aspect ratio and feature width as inputs and output an etch rate, as shown in Figure 4-3. This etch rate can then be integrated in a time-stepping simulation to predict etch depth for a given etch time.
Upon further careful examination, however, it is seen that the three input variables cannot be considered independently. In fact, both pattern density and feature width can be written in terms of aspect ratio.

The fundamental principles behind this model are similar to the pattern density model presented in Chapter 3. Specifically, we assume an inverse relationship between pattern density and etch rate. Several groups have shown that a relationship between ARDE and pattern density exists for DRIE [13]. However, pattern density needs to be redefined for this new case. In previous chapters pattern density referred to the ratio of bare vs. masked area on the wafer surface (i.e from a “top-down” viewpoint). Now we define $\gamma$, the surface loading fraction, as the ratio of bare to masked surface area of the wafer. Furthermore, $\gamma$ needs to be limited to a certain area of interest around a feature, perhaps the area corresponding the grid size used in the pattern density model. The loading fraction will actually increase over time, reaching one as time approaches infinity. The model is summarized below:

$$ER_t = \frac{C}{\gamma_t}$$  \hspace{1cm} (5.1)
where $C$ is the blanket etch rate and $\gamma_1$ is the newly-defined surface area loading fraction.

The expression breaks down for low aspect ratios ($\alpha < 1$). The expression for $\gamma_1$ is related to a feature’s geometry; for a rectangular slit it is defined as

$$\gamma_1 = \frac{\rho_o A_o + \beta(2\alpha h_1 h_2 + 2\alpha h_1^2)}{A_o + \beta(2\alpha h_1 h_2 + 2\alpha h_1^2)} \quad (5.2)$$

where $A_o$ is the area corresponding to the window of interest, $\alpha$ is the current aspect ratio of the feature and $\rho_o$ is the pattern density extracted from the layout. The numerator keeps track of the total exposed surface area as the aspect ratio increases, while the denominator is an expression for the total surface area, which also increases with increasing aspect ratio. Although it is now possible for the fluorine radicals to react with the sidewalls, it is still more likely for them to react with the bottom of feature. The dimensionless weighting constant $\beta$ is included in the equation for this reason.

![Figure 4-4 – Diagram of trench described in Equation 5.2](image)

### 4.3 Experimental Validation

We seek to validate the sidewall loading model through the use of an ARDE test mask. The goal of the experiment is to verify that the relationship between aspect ratio
(pattern density) and etch rate is consistent with the sidewall loading model, as well as to fit the empirical parameters $C$ and $\beta$ defined in the previous section.

The ARDE test mask was designed with a wide array of feature sizes and shapes in hope of mimicking the sometimes unusual structures used in MEMS. The dies include rectangular slits, circles, triangles, squares, and other shapes. Several dies featured rectangular slits 2 mm long and of varying widths. By measuring features on three different dies throughout the wafer, data was obtained for aspect ratios ranging from 1 to nearly 10. A diagram showing the location of the dies of interest is given below in Figure 4-5. The AutoCAD layout for the mask for is given in Figure 4-6.

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>H200 (fill)</td>
<td>H200 (fill)</td>
<td>G10</td>
<td>H200 (fill)</td>
<td>H200 (fill)</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>H200 (fill)</td>
<td>H200</td>
<td>L10</td>
<td>L200</td>
<td>H200</td>
<td>Triangles</td>
<td>H200 (fill)</td>
</tr>
<tr>
<td>3</td>
<td>H200 (fill)</td>
<td>Triangles</td>
<td>L100</td>
<td>Squares</td>
<td>H1_2.6mm</td>
<td>H100</td>
<td>H200 (fill)</td>
</tr>
<tr>
<td>4</td>
<td>H200</td>
<td>H50</td>
<td>Exposure</td>
<td>H400</td>
<td>Squares</td>
<td>L200</td>
<td>H200</td>
</tr>
<tr>
<td>5</td>
<td>H200 (fill)</td>
<td>Squares</td>
<td>H3_4.5mm</td>
<td>L200</td>
<td>L400</td>
<td>H200</td>
<td>H200 (fill)</td>
</tr>
<tr>
<td>6</td>
<td>H200 (fill)</td>
<td>H150</td>
<td>L50</td>
<td>Triangles</td>
<td>L20</td>
<td>H800</td>
<td>H200 (fill)</td>
</tr>
<tr>
<td>7</td>
<td>H200 (fill)</td>
<td>H200 (fill)</td>
<td>G5</td>
<td>H200</td>
<td>G20</td>
<td>H200 (fill)</td>
<td>H200 (fill)</td>
</tr>
</tbody>
</table>

Figure 4-5 – Die map for ARDE test mask.
Structures on the L10, L20, and L50 dies were measured. Each of these dies contains an array of rectangular slits, varying in width from 0/+17 µm of their nominal value.

The samples were prepared by first growing 1.4 µm of thermal oxide on blank wafers. A thick oxide layer is needed to weather damage done by ion bombardment during the DRIE process. Following oxidation the wafers were coated with 10 µm of thick resist (AZ4620). Following an 20 second exposure (after a 1 hr prebake) with the EV1 contact aligner and 135 second development with AZ440 developer, the wafers were ready for the DRIE step. Six wafers were etched in an STS Inductively Coupled Plasma Etcher ICP at increasingly longer time intervals (10, 20, 30, 40, 50, and 60 minutes, respectively). The wafer orientation was kept constant for each wafer in order to minimize any interference from wafer-level effects. Additionally, the wafers were processed on the same day to avoid problems with etch-rate drift in the tool. After the DRIE step, the
photoresist was removed by ashing in an oxygen plasma, followed by an HF dip to remove the oxide layer.

Figure 4-7 – SEM image of 10 µm trench etched for 50 minutes. The measured feature width was 11.3 µm. Additionally, the trench appears to be slightly angled from the wafer normal.

Figure 4-8 – SEM image of 10 um trench etched for 40 minutes. Debris is clearly visible on the surface and sidewall.

After the processing steps, the widths and depths of each trench were recorded for each time step. The larger feature widths (>10 µm) were measured with the WYKO
profilometer. It was not possible to measure the 10 µm and smaller trenches with the WYKO; cross sections were measured using a scanning electron microscope (SEM). There was a marked difference in sample cleanliness before and after the diesaw step; an instance of debris in a trench is shown in Figure 4-8. SEM measurement revealed significant process variation with respect to the trench width on the L10 die. While we expected them to be 10 µm, the actual widths varied from 11-13 microns. This discrepancy can be explained by processing error (i.e., overexposure and overdevelopment) during the lithography step. The measured widths values were used to calculate aspect ratios. Table 4-1 below contains the data for each of the time steps.

**Table 4-1 – Data obtained for rectangular slits for each time step.**

<table>
<thead>
<tr>
<th>nominal width (µm)</th>
<th>time (min)</th>
<th>depth (microns)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>10</td>
<td>22</td>
<td>40.5</td>
</tr>
<tr>
<td>20</td>
<td>24.25</td>
<td>41.88</td>
</tr>
<tr>
<td>30</td>
<td>24.52</td>
<td>43.68</td>
</tr>
<tr>
<td>35</td>
<td>25.27</td>
<td>44.56</td>
</tr>
<tr>
<td>50</td>
<td>23.29</td>
<td>44.91</td>
</tr>
<tr>
<td>60</td>
<td>21.99</td>
<td>45.34</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>nominal width (µm)</th>
<th>time (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>10</td>
</tr>
<tr>
<td>10</td>
<td>12.5</td>
</tr>
<tr>
<td>20</td>
<td>19.9</td>
</tr>
<tr>
<td>30</td>
<td>31.2</td>
</tr>
<tr>
<td>35</td>
<td>34.4</td>
</tr>
<tr>
<td>50</td>
<td>52.7</td>
</tr>
<tr>
<td>60</td>
<td>63.9</td>
</tr>
</tbody>
</table>
Although data was obtained at six time steps for each nominal width, only the data from the 10 µm trenches was used to fit the model. Since the rest of the data was taken using the WYKO, there was more error in it. Furthermore, these trenches yielded the largest range in aspect ratios. The plot in Figure 4.8 shows the best empirical fit for Equation 5.1. In order to fit the sidewall loading model, the pattern density window of interest was chosen as 100 µm x 100 µm. As a result \( h_1 \) and \( h_2 \) are 10 and 100 µm rather than 10 µm and 2000 µm. The constants \( C \) and \( \beta \) were fit to 1.45 and 3.98 respectively. It is clear from Figure 4.8 that the function \( ER_1 \) will only fit the data in the Knudsen transport regime; the predicted ER is far too high in the reaction rate limited regime \( (0 < \alpha < 1) \). Fortunately, most high aspect ratio features of interest used in MEMS will fall into this range. For low aspect ratio structures, we can assume the etch rate is equal to the ER for an aspect ratio of 1. For extremely high aspect ratios, we assume etching stops.

![Comparison with experimental data for sidewall loading model](image)

**Figure 4-9 – Comparison between data and sidewall loading model from 10um trenches.**
The critical aspect ratio is marked with a dotted line. The blue curve represents function \( ER_1 \).

To summarize, the sidewall loading model can be described by equation 5.3.
For this set of data, the sidewall loading model was also compared to the Coburn-Winters model presented in Chapter 2. Figure 4-10 is a plot of the best fit of the Coburn-Winters model to the 10 µm trenches. \( R_0 \), the etch rate as the aspect ratio approaches zero, was found to be 2.64 µm per minute. The sidewall loading model predicts an initial etch rate of 2.8 µm/min. \( S \), the molecular reaction probability, was fit to 0.27. The normalized RMS error for the Coburn-Winters fit was 5.8% for the data; it was 6.1% using the sidewall loading model. Although the errors for both models are of the same order of magnitude, the structure of the sidewall loading model will allow it to be easily integrated into the pattern density model described in Chapter 3.

\[
ER = \begin{cases} 
ER_0(\alpha = 1), & \alpha \leq 1 \\
ER_1, & 1 \leq \alpha \leq 25 \\
0, & \alpha \geq 25 
\end{cases}
\]  

(5.3)
4.4 Future Work: Integration into a time-stepping etch rate model

Now that an analytical equation relating etch rate with respect to aspect ratio has been obtained, it can be used in concert with the pattern density model in chapter 3 to produce a time-stepping etch rate model. The flowchart in Figure 4-11 outlines the framework of such a model. The first step is obtaining a line-width extraction for the layout. This extraction can be obtained using tools from Praesagus, which also provides density extractions for the pattern density model. In order to obtain true aspect ratio data, the grid size for the line-width extractions needs to correspond to the maximum feature size for

![Flowchart describing the flow of a time-stepping etch model.](image-url)
the particular layout. Next, three matrices corresponding to the layout need to be created: one for holding the aspect ratio data, another for holding the depth at each point, and a third holding the instantaneous etch rate. The aspect ratio and the depth matrices can have every unmasked point initialized to zero, and each masked grid point set to NaN. After assigning an appropriate etch rate for each point, the etch rate matrix can be normalized by the pattern density map (i.e., the output of the model described in chapter 3) via multiplication. This result can be multiplied by \( \Delta t \) to calculate the change in depth; the result is added to the depths matrix. Finally, the process repeats until etching is complete.

### 4.5 Summary

The following chapter presented a sidewall loading model to predict aspect-ratio dependent etching. A calibration of the model using data from etched rectangular slits was described. Finally, a brief comparison with the Coburn-Winters ARDE model was made.
Chapter 5

Filling Strategies for Uniformity Improvement in DRIE

This chapter will present some of the strategies being explored to improve uniformity in DRIE. Specifically methods for synthesizing and placing dummy features in a layout will be discussed.

5.1 Background

Much of the previous work surrounding dummy filling and slotting has focused on the planarization step in IC fabrication (CMP) [16]. A promising idea for improving DRIE uniformity is the insertion of dummy fill into a mask layout. These new structures would balance out loading density across the wafer, resulting in a more uniform etch. Dummy fill has been extensively studied at the die level for CMP. Filling methods can be classified into two methods: rule-based and model-based. Rule-based filling involves adding a repeating pattern to the un-etched parts of the mask. Model-based filling involves using integer programming to optimize the pattern density, and results in a fill design more specifically tailored to the mask. It is important to note the difference between filling and slotting. Filling refers to placing extra structures into a layout. Slotting refers to etching extra features out of a pattern. Both methods have been demonstrated for CMP by Chen et al. [15]. Figure 5-1 describes dummy fill as it is generally implemented in the integrated circuit industry. The upper left image represents the unfilled IC layout. Note that all of the features are rectangular. The situation in MEMS is substantially different. The dotted lines represent exclusion zones specified by the designer, where no fill can exist. The upper right image represents an array of periodic metal fill. These fill patterns are generally placed in areas with very low pattern
densities. In Figure 5-1 (c), the layout in (a) and the fill pattern in (b) have been merged using a logical operation. This step is typically done using layout manipulation tools, such as those provided in Cadence or other CAD suites. Figure 5-1 (d) shows how fill can be optimized in the model-based fill approach.

Figure 5-1 - (a) IC layout (b) array of rule-based fill (c) logical overlay of layout and rule-based fill (d) implementation of model-based fill [16].

Although it is generally accepted that model-based filling provides more balanced pattern density, both methods are used in industry. The problem for DRIE is slightly different than CMP, in that in many cases we are unable to place features directly into the die. For MEMS, any placement of features within the die would have to be coordinated with the designer. Also, electrical capacitance created by CMP fill is not an issue for DRIE. However, having large etched areas on the wafer could affect wafer bonding.
5.2 Test Mask

To examine the effect of placing uniform dummy fill around a die, two test masks were created. Each of them features a test die consisting of lines and spaces, as shown in Figure 5-2.

![Diagram describing dummy fill test die.](image)

**Figure 5-2** – Diagram describing dummy fill test die.

![Test die with a 50% fill ring (shaded).](image)

**Figure 5-3** – Test die with a 50% fill ring (shaded).
Although the pattern densities in the quadrants range from 25% to 75%, the overall loading for the die is 50%. One mask featured a single die in the upper left hand corner, while the second mask featured the die with a 5 mm fill ring surrounding it, as shown in Figure 5-3. A 1 mm exclusion zone was placed between the die and fill ring. Both masks had monitor points covering the rest of the surface to capture wafer-scale variation.

5.2.1 Simulation

Both masks were simulated using the die-level block of the pattern density model described in Chapter 3. Only the die-level block is used because the goal of filling/slotting is to make the pattern density as uniform as possible. Figure 5-4 illustrates the effect of die-level interaction on the test die without any fill surrounding it.

![Simulation for die without fill](image)

Figure 5-4 – Pattern Density Simulation for test die. The color scale represents normalized etch rate.

As expected, the pattern density model suggests that the quadrant with the highest pattern density will experience the lowest etch rate. The same simulation was performed for the die surrounded by the 50% fill ring; the result is plotted in Figure 5-5 below. Examination of the simulation result suggests that microloading is still present after the uniform fill
ring is implemented. A slight improvement in normalized etch rate range is seen, as well as a reduction in the overall etch rate due to increased loading.

5.3 Experiment

This conclusion is further supported by experimental data. The test die described above was etched both with and without the fill rings. A short process flow consisting of 30 minutes of etching with 1.4 µm of thermal oxide and 10 µm of thick resist for a hard mask was used. Figure 5-6 and Figure 5-7 show normalized results from each of the etches. The data plotted is a spatial representation of the normalized average etch rate for the bottom of each feature. Though it is unaccounted for in the pattern density simulation, the effect of ARDE is seen via discontinuities in etch rate. The increase in etch rate near the die edges in both figures indicate that pattern density effects are still present. However, when data is taken across a line in the center of the upper left quadrant (Figure 5-8), it is clear that the microloading effect has been slightly reduced.

Figure 5-5 - Pattern Density Simulation for test die with a uniform fill ring. The color scale represents normalized etch rate.
Figure 5-6 – Normalized results for test die without fill.

Figure 5-7 – Normalized results for test die with 50% fill ring.
Figure 5-8 – Comparison between experimental data (circles) and model (line) for the test die with and without fill.

The experiment described above suggested that asymmetric dummy fill might provide a better method of reducing die-to-die interaction. The following section describes the methodology and results of such a pattern fill scheme.

5.4 Methodology for Optimized Dummy Fill

Dummy fill features can be synthesized through the use of the pattern density model in conjunction with the optimization functions available in MATLAB. The first step is to identify where to place the features in the layout. Due to the sparseness of most MEMS layouts, these “fill zones” can simply be the bare areas of the wafer. By contrast, an initial density analysis is needed to determine the fill zones for integrated circuit layouts (which are much more dense). Next, the fill zones need to be partitioned into tiles to be individually optimized to a specific pattern density. To simplify the process, any existing symmetries in the layout should be taken advantage of. In practice, the fill zones should be selected to add minimal loading to the layout, so as not to affect other process steps (especially wafer bonding). Once the pattern densities for each tile have been obtained
they can be implemented in any number of ways; lines and spaces are best since they will cause minimal increase in the size of the CAD layout file. When optimizing the fill zones, it is important to ensure that the tile values are properly constrained (they must be positive, and less than 1). This can be accomplished by taking the absolute value of the tile values before their insertion, and adding a large penalty value to the objective function if tile values greater than 1 exist. The optimization works by picking density values for a block, calculating the etch rate perturbation using the pattern density model, and then evaluating a specified objective function. Here we use the variance in normalized etch depth across a specified set of locations within the die; It is this quantity that will be minimized during the optimization. In order to speed up the optimization process, the convolution operation in the pattern density model was executed via a two-dimensional FFT.

![Figure 5-9 – Illustration of a fill zone partitioned into tiles and a possible objective function.](image)

Figure 5-9 – Illustration of a fill zone partitioned into tiles and a possible objective function.
5.5 **Optimization of the Turbopump Layout**

Fill zones for dummy fill were optimized for the turbopump layout that is described in Chapter 3. Several different fill schemes were evaluated. The first scheme allows for fill in the areas surrounding the outer dies; the second scheme utilizes the areas between the dies for fill structures.

5.5.1 *Edge Fill*

The layout in Figure 5-10 consists of 11 4 mm x 4 mm tiles adjacent to each of the edge dies, for a total of 44 tiles. Since the center die already had uniform loading around it, we decided that an adjacent fill zone was not necessary. This scheme makes use of the radial symmetry of the layout; 11 tiles are optimized and repeated rather than all 44. Each tile was given a starting pattern density of 50% before the optimization began. For an objective function, the variance at a 2.2 mm radius from the center of the upper left die was minimized using the fminsearch function in MATLAB.

![Figure 5-10 – Turbopump Layout with fill zones before optimization.](image)
Figure 5-11 – Turbopump Layout after optimization.

Figure 5-11 illustrates the layout after the optimization process. The tiles only add about 1% of loading to the wafer-level pattern density, so the overall etch rate of the filled design should be similar to the original. The actual tile densities are shown in Figure 5-12.

Figure 5-12 – Closeup of upper left optimized die with labeled tile values.
Comparison of the objective function for the mask with and without fill shows significant improvement in the uniformity for the outside dies. Variance values of normalized etch rate before and after the optimization are given in Table 5-1. Additionally, Figure 5-13 to Figure 5-17 compare the objective function data for layouts with and without edge fill for each die. The data is normalized in the same manner as Figure 3-19.

Table 5-1 – Variance data for optimization with edge fill.

<table>
<thead>
<tr>
<th>Die</th>
<th>( \sigma^2 ) without fill (dimensionless)</th>
<th>( \sigma^2 ) with fill (dimensionless)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4.32x10^{-6}</td>
<td>6.83x10^{-7}</td>
</tr>
<tr>
<td>2</td>
<td>5.03x10^{-6}</td>
<td>6.30x10^{-7}</td>
</tr>
<tr>
<td>3</td>
<td>4.61x10^{-7}</td>
<td>4.61x10^{-7}</td>
</tr>
<tr>
<td>4</td>
<td>4.78x10^{-6}</td>
<td>5.28x10^{-7}</td>
</tr>
<tr>
<td>5</td>
<td>4.31x10^{-6}</td>
<td>6.5x10^{-7}</td>
</tr>
</tbody>
</table>

Figure 5-13 – Comparison of objective function data with and without fill for upper left die.
Figure 5-14 - Comparison of objective function data with and without fill for upper right die.

Figure 5-15 - Comparison of objective function data with and without fill for center die. In this case, little difference between the two cases is observed.
Figure 5-16 - Comparison of objective function data with and without fill for lower left die.

Figure 5-17 - Comparison of objective function data with and without fill for lower right die.

Figure 5-18 shows the across-die variation with fill for the lower right die. The etch behavior is noticeably more uniform than its counterpart without fill, which is given in Figure 3-16.
5.5.2 Other Objective Functions

There are an array of other objective functions that could be used to synthesize the filled tile values. No matter what function is used, it is important that it has some sort of symmetry with all dies on the wafer. One specific objective function that was evaluated featured the minimization of variance of a 21-point cross pattern across the upper left die. For this objective function the edge fill zones were used. An image of the resulting layout is provided in Figure 5-19. Comparison of Figure 5-20 and Figure 5-18 suggests that this collection of points is a slightly better choice than the ring used earlier; the variance for the selected points on the upper left die was 3.5x10^-7.

Figure 5-18 – Across die variation for lower right die with optimized fill.
Figure 5-19 – Turbopump layout after optimization with cross objective function.

Figure 5-20 – Across die variation for lower right die using cross objective function.

5.6 Limitations

There are several limitations to the iterative synthesis method described above. Foremost of these is the required computing time. The optimization of 11 tiles took several hours to complete, so using smaller tiles will increase the required time substantially. Also, iterative optimization is much more likely to get stuck in a
locally optimal solution if there are a high number of variables. Additionally, an iterative solution is heavily dependent on the initial values of the optimization variables. A better approach may be to use the simulated annealing algorithm described by Kirkpatrick et al. [17]. Instead of only accepting changes in tile values that improve the objective function (as is done in iterative optimization), tile changes that worsen the objective function may also be accepted according to a probability function. Kirkpatrick formulates the probability function as having an exponential dependence on inverse “temperature;” by “cooling” this value an optimal solution can be approached. This method could certainly be applied to layout optimization; it has already successfully been applied to circuit placement and wiring [17].

5.7 Summary

This chapter presented several methods for inserting dummy fill features into a MEMS layout in hopes of improving uniformity. An experiment was described which evaluated the effects of uniform fill around the die. Later, an algorithm for optimizing fill features was described and simulated for the turbopump layout. Edge tiling of the fill zones was more effective than block tiling. The level of improvement seems to depend on what points are chosen for the objective function. Lastly, the limitations of the current optimization method and a possible future direction were described.
Chapter 6

Conclusions and Future Work

This thesis has presented a model which can predict normalized etch rate uniformity based on the pattern density of a given layout. Also, methods to synthesize dummy features using the model were outlined.

6.1 Pattern Density Model

A pattern density based model has been presented for spatial mapping of layout dependent effects in DRIE. The accurately predicts large across-die variations (6-7%) existing in DRIE applications. The model can also capture subtle within-die effects, with additional tuning to within 0.1% (normalized RMS error) of accuracy.

6.2 Sidewall Loading Model

A sidewall loading model, which tracks instantaneous etch rate as a function of aspect ratio, was proposed. Data from the ARDE test mask was fit to the model with an error of 6.1% (normalized RMS); the normalized fit for the Coburn-Winters model was 5.8%. Although the errors for both models are of the same order of magnitude, the structure of the sidewall loading model will allow it to be easily integrated into the pattern density model described in Chapter 3. The integration of these two model can eventually lead to a time-stepping etch rate model based on pattern density, as discussed in Chapter 4.

6.3 Synthesis of Dummy Features

Chapter 5 presented several methods for inserting dummy features into a layout in hopes of improving uniformity. An experiment was described which evaluated the effects of uniform fill patterns across the die. Later, an algorithm for optimizing fill features was described and simulated for the turbopump layout. Edge tiling of the fill zones was more
effective than block tiling. It was shown that edge tiling improved the variance of our chosen objective function by an order of magnitude. Lastly, the level of improvement seems to depend on what points were chosen for the objective function.

6.4 Future Work

There are many possibilities for future work in all three of the areas summarized above. For the die-level model, alternative functional forms for the pattern density filter function (e.g. $1/r^b$) may be considered, or may apply in different etch circumstances. Perhaps a finite-element modeling tool (such as FEMLAB or ANSYS) could be used to explore or develop an alternative analytic expression for the filter function. Finally, alternative ways of combining these three components (e.g. in a multiplicative rather than additive manner) can be considered to account for interaction between wafer-, die-, and feature-level effects. Another exciting avenue of future work is the integration of sidewall loading and pattern density models to create a model that predicts absolute etch rate with respect to time.

In the area of dummy feature synthesis, one significant barrier in the optimization process is the run time of the MATLAB minimization function; it seemed to increase exponentially with the number of optimization variables. One way to synthesize more complex structures on a smaller grid size would be to use a more efficient algorithm such as “simulated annealing” rather than the iterative optimization functions provided in MATLAB.

In conclusion, this thesis contributes a framework towards predicting and improving uniformity in deep reactive ion etch.
References


