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Inter- and intra-die polysilicon critical dimension variation

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ABSTRACT

A methodology has been developed as part of a statistical metrology framework (1) to assess the relative range and distribution of intra-die, or die-level, polysilicon critical dimension variation as opposed to wafer-level, or inter-die, poly-CD variation; (2) to identify the key layout factors involved in poly-CD intra-die variation; and (3) to develop first-order semi-empirical models for poly-CD variation. A new approach utilizing multivariate analysis of variance methods is described to model the die- and wafer-level variation components. We show that pattern dependent variation is approximately twice as large as wafer-level variation. In addition, we find that spatial position plays a strong role: the first-order pattern dependent variation model (or die "signature") shows a strong dependence on spatial position across the wafer, and individual components of the model demonstrate different spatial position sensitivities.

Keywords: polysilicon critical dimension, variation, statistical metrology, intra-die variation, spatial modeling

1. INTRODUCTION

As device and interconnect dimensions continue to scale towards tenth-micron dimensions, maintaining process uniformity and compensating for deeply confounded interactions at each processing step is increasing in importance and complexity. With the primary exception of high-precision analog applications, the impact of variation on circuits designed and fabricated using previous process technologies based on one micron or larger features has been relatively minor. As the feature size has approached half-micron dimensions and the wafer size has grown to 200mm, the detrimental impact of variation has begun to assume a more prominent position. This is mainly attributed to a shrinking of feature dimensions without a corresponding increase in machine precision and tolerance. New methods are needed understand and manage variation in emerging technologies.

1.1 Motivation

"Worst-case" based approaches to coping with variation are often inadequate or highly conservative especially for key parameters such as the polysilicon critical dimension and the intra-level dielectric thickness which have a direct impact on circuit performance. In addition, "worst-case" based design rules do not allow the circuit designer to trade performance for reliability and *vice-versa* in that it is impossible for a circuit designer to know *a priori* which design rule violations are the most destructive and which are only slightly destructive in the sense of yield. Because of these limitations, methods are needed to characterize and model variation as an enabling tool for accurate simulation and process/device/circuit modeling.

The design of high speed integrated circuits must account for variation in the devices and interconnect within the circuit. Traditionally, this has been accomplished by way of design rules which govern the shape and proximity of various layout structures, and worst-case/best-case device model (SPICE) files. For analog circuitry, careful attention to the matching of devices within the circuit is required, while digital designers have proceeded comfortable in the belief that variation within the circuit will be small and not disturb digital operation. As clock speeds have increased, however, the importance of device and interconnect variation in limiting performance has increased. Furthermore, the relative magnitude of manufacturing variation is increasing. To continue technology and circuit performance improvements, manufacturing variation and its impact on high performance VLSI circuits must be better understood.

Poly-CD variation is especially important. Variation in the polysilicon critical dimension, or poly CD, translates directly into MOS transistor channel length variation. Current lithography and etch technology can typically achieve wafer-scale line width uniformity of approximately 5% (measurements of the same structure within each chip across the wafer). Design typically assumes that the variation within any one chip will be smaller than this. However, measurements of supposedly identical structures within the same die reveal variations on the order of 15%. Clearly, additional physical effects are coming into play at this scale, such as pattern dependencies during etch or systematic lens distortions in photolithography. The modeling of spatial variation not only across the wafer, but also intra-die, is of critical concern for circuit performance and manufacturability.

Intra-die variation is often caused by layout and topography interaction with the process. Key examples include critical line-width dimension variation in channel length or metal lines [1, 2, 3], and pattern planarization in chemical mechanical polishing [4, 5]. Intra-die variation has only recently received appreciable attention, in part due to the need for a large amount of statistically meaningful data, and the prevailing belief that intra-die variation is inconsequential compared to lot-to-lot, wafer-to-wafer, and within-wafer variation. Our studies [4, 6] and those elsewhere [1, 3] have shown that this is not the case and that intra-die variation is often much larger or comparable to the other variational sources.

1.2 Statistical Metrology

In order to assess and model poly-CD variation, we utilize and extend an emerging "statistical metrology" methodology. Statistical metrology is a general methodology for understanding both temporal and spatial parameter variation. The parameters of concern may be structural (e.g. dimensions of features) or electrical (e.g. transistor or interconnect performances). There are three main phases of statistical metrology: variation assessment, variation modeling, and variation impact. In variation assessment, the primary goal is to understand the source and extent of variation in the sense of answering the questions *where?* and *how much?* In particular, *where* is the most amount of variation centered? Is it intra-die, wafer-level, or wafer-to-wafer variation? *How much* of the total variation is attributed to wafer-level, intra-die, wafer-to-wafer, etc.? In the variation modeling phase of statistical metrology, the primary goal is to model any systematic variation, either at the wafer-level or die-level, as a function of either layout/pattern factors (in the case of die-level variation) or processing parameters (usually in the case of wafer-level variation) through the use of traditional or modified ANOVA or other statistical modeling techniques. Finally, in the impact phase of statistical metrology, the primary concern is understanding the relationships between parameter variation and the resulting circuit performance and manufacturability or yield.

1.3 Organization of the paper

In this paper, methods are contributed for the assessment and modeling of spatial and pattern-dependent variation, with application to the study of polysilicon critical dimension in order (1) to assess the relative range and distribution of intra-die, or die-level, polysilicon critical dimension variation as opposed to wafer-level, or inter-die, poly-CD variation; (2) to identify the key layout factors involved in poly-CD intra-die variation, and (3) to develop first-order semi-empirical models for poly-CD variation. Unlike previous research where special short flow masks were utilized [1, 2], this work is conducted on a full flow process with devices in a realistic circuit environment; this experimental methodology is described in Section 2. Novel statistical analysis techniques for variation modeling are described in Section 3 which overcome limitations in previous spatial frequency approaches [1, 7]. The analysis of poly-CD variation using this modeling technique is then presented in Section 4. Finally, conclusions are offered in Section 5 regarding poly-CD variation and the potential application of the methodology to other variation concerns such as interconnect or threshold voltage variation.

2. EXPERIMENTAL METHODOLOGY

Since a large volume of statistically significant data is required, direct optical measurement of poly-CD is impractical. An early attempt at using optical/SEM techniques resulted in an excessively low throughput [8]. For this reason, electrical measurement techniques are desired. An independent experiment based on simulation and physical measurements revealed that the majority of Id_{sat} variation is attributable to poly-CD variation as opposed to threshold voltage variation and substrate doping concentration distributions. We thus use Id_{sat}, the measured drain current when the gate and drain are connected to the power supply and the source is grounded (for NMOS), as a metric of poly-CD variation. A set of 27 NMOS transistors with a nominal channel length of 0.35μm and various layout factors including gate width, geometric orientation, spatial location, and presence or absence of neighboring structure were selected from a standard test vehicle (see Table I). Every die on twelve wafers from two different lots were probed to yield over 16,000 observations.

Table I. Transistor Layout Factors

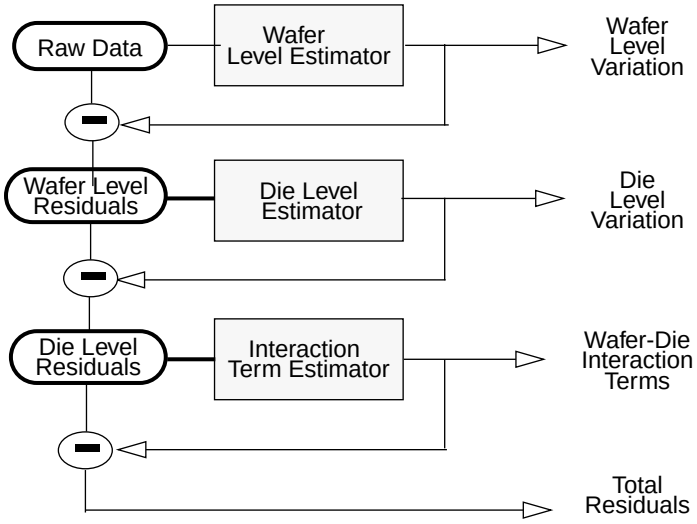
Number of Transistors	Geometric Orientation	Spacing	Width
5	Horizontal	Fingered	14 μm
7	Horizontal	Isolated	14 μm
1	Horizontal	Isolated	9 μm
2	Horizontal	Stacked	14 μm
4	Vertical	Fingered	14 μm
7	Vertical	Isolated	14 μm
1	Vertical	Isolated	9 μm

3. VARIATION DECOMPOSITION AND MODELING

Because the physical sources of spatial variation at the wafer- and die-levels are very different, it is critical that methods be available for the separation and analysis of variation components. Equipment and process-related issues can then be identified and addressed via process optimization and control, and pattern dependencies can be minimized by judicious circuit design practices.

Figure 1 shows a flow diagram for the general decomposition algorithm. A hierarchical model is assumed in which the residuals (the output of the previous estimator minus its input) from one estimator becomes the input to the next estimator. There are three main estimators depicted in Figure 1: the wafer-level estimator, the die-level estimator, and the wafer-die interaction term estimator. The final box in Figure 1 represents the residual terms -- the portion of the variation that is left over and assumed to be purely random in nature.

Figure 1. Variation Method Flow Diagram



Generally speaking, the variation decomposition algorithm can be expressed in the framework of an additive model. An excellent discussion of generalized additive models, of which we use a special case, can be found in [9, 10]. Using an additive model allows the total variation to be expressed as the sum of other variation terms such as die-level variation, wafer-level variation, and die-cross wafer level variation.

$$f_{RAW} = f_{WLV}(x, y) + f_{DLV}(x, y) + f_{WLV \otimes DLV}(x, y) + \varepsilon \quad where \quad \varepsilon \sim N(0, \sigma^2) \tag{1}$$

In (1), *x* and *y* are spatial coordinates on the wafer while f_{WLV} is the wafer-level variation, f_{DLV} is the die-level variation, and $f_{WLV \otimes DLV}$ represents the wafer-die interaction terms. Here ε corresponds to the residual terms mentioned before.

3.1 Wafer level estimator

In this paper, a regression approach is used to extract the wafer-level variation. In this estimator, the wafer-level variation is assumed to be a smooth function of *x, y, r,* θ, or other relevant coordinates. The estimator used here is of the form:

$$f_{WLV} = \alpha_0 r + \alpha_1 r^2 + \alpha_2 x + \alpha_3 y + \alpha_4 xy \tag{2}$$

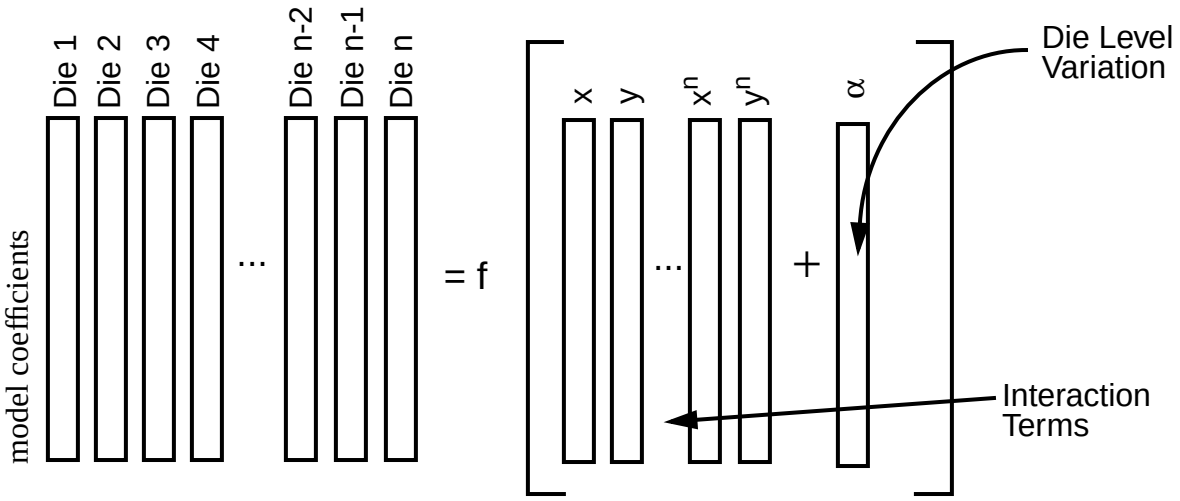
where standard least squares regression to the available data is employed. Other estimation techniques and procedures as well as a comparison of the relative efficiency of each technique can be found in [7].

3.2 Die level estimator

Because the data used in this study come from a full-flow experiment and the spatial positions of each structure are only known to a coarse degree of accuracy, the standard techniques discussed in [7] cannot be used to estimate the die-level and wafer-die interaction terms shown in Figure 1. Instead, a modified ANOVA approach (first introduced in [6]) is developed and applied here.

A “VarNOVA” procedure (VARiation modeling using aNalysis Of VAriance) has been developed to estimate die-level variation and wafer-die-interaction components for use in highly confounded environments, e.g. full-flow designs, or in cases where every die has not been measured (all die are needed in the frequency based approaches presented in [1, 7]). The process begins by developing an ANOVA model for each die measured as a function of the designed layout factors (e.g., Table I). The model coefficients as well as the spatial coordinates of each die are assembled together. These model coefficients are then regressed onto a polynomial function of the spatial coordinates of each die usually using a MANOVA technique. The constant terms (which are independent of the die spatial coordinates) thus form the die-level (or intra-die) component of the model, while those which are a function of the die coordinates form the wafer-die interaction components. The remaining terms become the residual components.

Figure 2. The VarNOVA Procedure

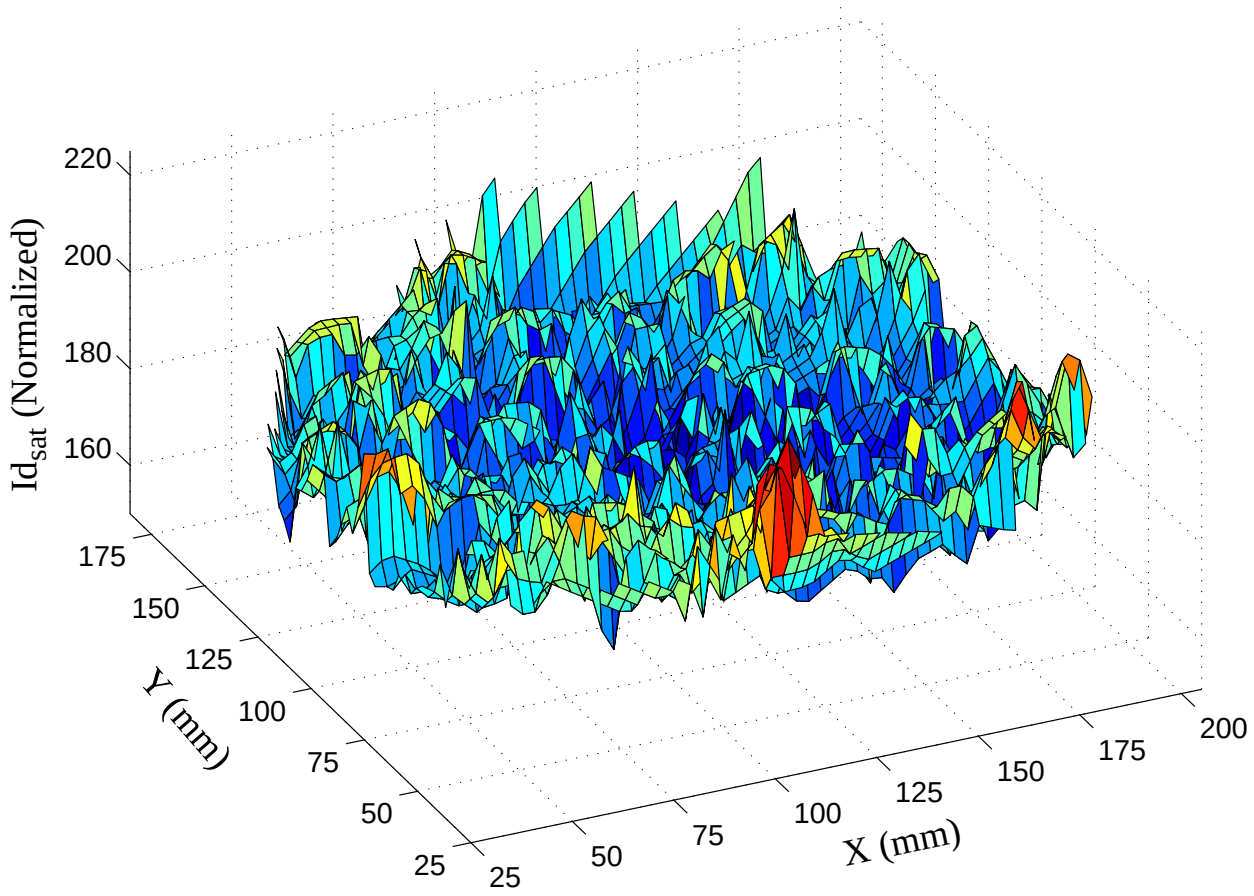


4. POLY-CD DATA ANALYSIS

In this section, the extracted components of poly-CD variation are presented for a sampling of the measured wafers. The estimators introduced in the previous section are used to extract the wafer-level, die-level, and wafer-die variation components. All measured current values have been arbitrarily normalized.

Figure 3 shows the raw data for one particular wafer. The smooth, low-frequency characteristics of the wafer-level components can be seen as well as local bumpiness associated with die-level and wafer-die interaction components of variation.

Figure 3. Raw Polysilicon Critical Dimension Variation for Wafer 17.



4.1 Wafer-level variation components

Figure 4 shows the extracted wafer-level variation components for four measured wafers. The upper two wafers come from Lot “A” while the lower two wafers come from lot “B”. The wafer-level extraction procedure detailed in Section 3 is used. In all the wafers, there is a clear radial dependence as well as a linear trend visible. Also, significant lot-to-lot and wafer-to-wafer variation is visible.

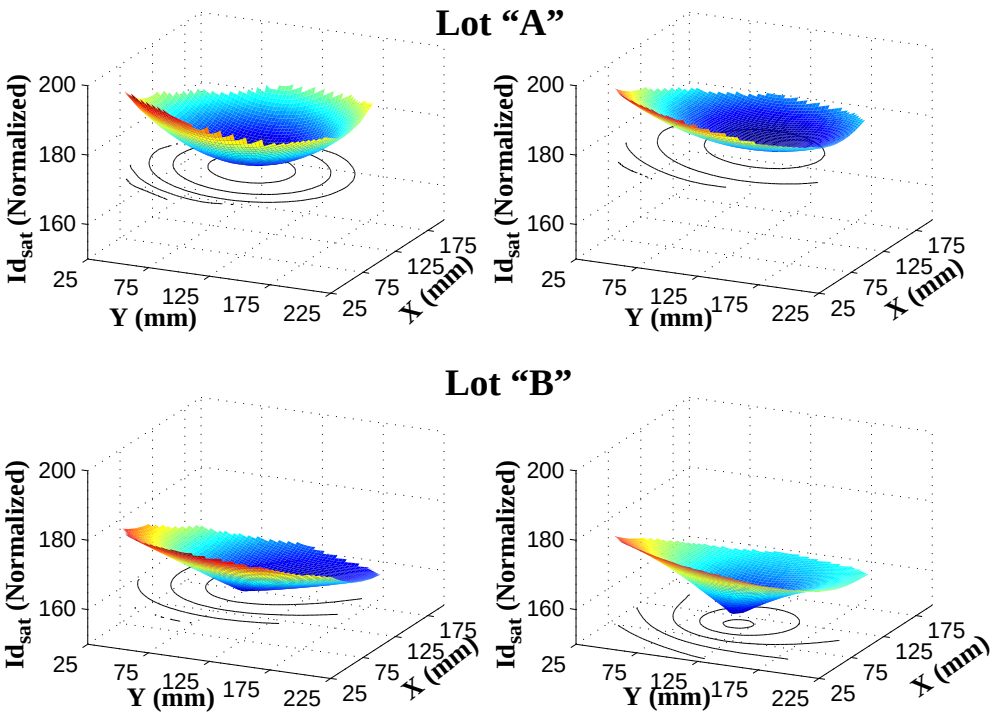
4.2 Die-level and wafer-die interaction terms

The techniques highlighted in Section 3 are used to extract a die-level and a wafer-die interaction term model. For each measured die, an ANOVA model:

$$Id_{SAT} = \mu + \begin{Bmatrix} \alpha_F \\ \alpha_I \\ \alpha_S \end{Bmatrix} + \begin{Bmatrix} \beta_H \\ \beta_V \end{Bmatrix} + \begin{Bmatrix} \gamma_{WIDE} \\ \gamma_{NARROW} \end{Bmatrix} \quad (3)$$

is developed. Since the design was unbalanced and research revealed that interaction terms added little to the quality of the model, interaction terms were neglected. In (3), μ, α_F, α_I, α_S, β_H, β_V, γ_{WIDE}, and γ_{NARROW} are constants which are fitted to the data. In this type of model, the expected Id_{sat} value for a particular transistor with a given set of layout factors is determined by selecting the appropriate constant term from each brace and adding each term together. For example, if a transistor is horizontally oriented, isolated, and wide, then the expected Id_{sat} value is $\mu + \alpha_I + \beta_H + \gamma_{WIDE}$. Also note that all of the models are fitted to the data with the wafer-level variation removed.

Figure 4. Several Extracted Wafer-Level Variation Components



A typical ANOVA model (normalized) for a die near the center of the wafer is:

$$Id_{SAT} = 0.409 + \begin{Bmatrix} 9.375 \\ 10.630 \\ 1.254 \end{Bmatrix} + \begin{Bmatrix} -3.162 \\ 3.162 \end{Bmatrix} + \begin{Bmatrix} -1.641 \\ 1.641 \end{Bmatrix} \quad (4)$$

and the ANOVA table for this particular die is shown in Table III. The ANOVA table reveals that spacing (fingered vs. isolated vs. stacked) and geometric orientation (horizontal vs. vertical) are the most significant layout factors while channel width is not significant as judged by the Pr(F) column (under a few assumptions of normality, there values indicate the probability that

the observed differences between groups could have arisen by chance alone). For this reason, the channel width layout factor is not included in any of the models presented below.

Table II. ANOVA Table for Wafer 21, Lot "A", Die 44.

Factor	DF	Sum of Sq.	Mean Sq.	F-value	Pr(F)
spacing	2	6964	3482	81.41	0.0000
geom. orient.	1	745.8	745.8	17.44	0.0003
width	1	56.8	56.8	1.32	0.2614
Residuals	22	940.961	42.77	-	-

Figure 5. The Spatial Dependence of the Model Coefficients for Wafer 21, Lot "A"

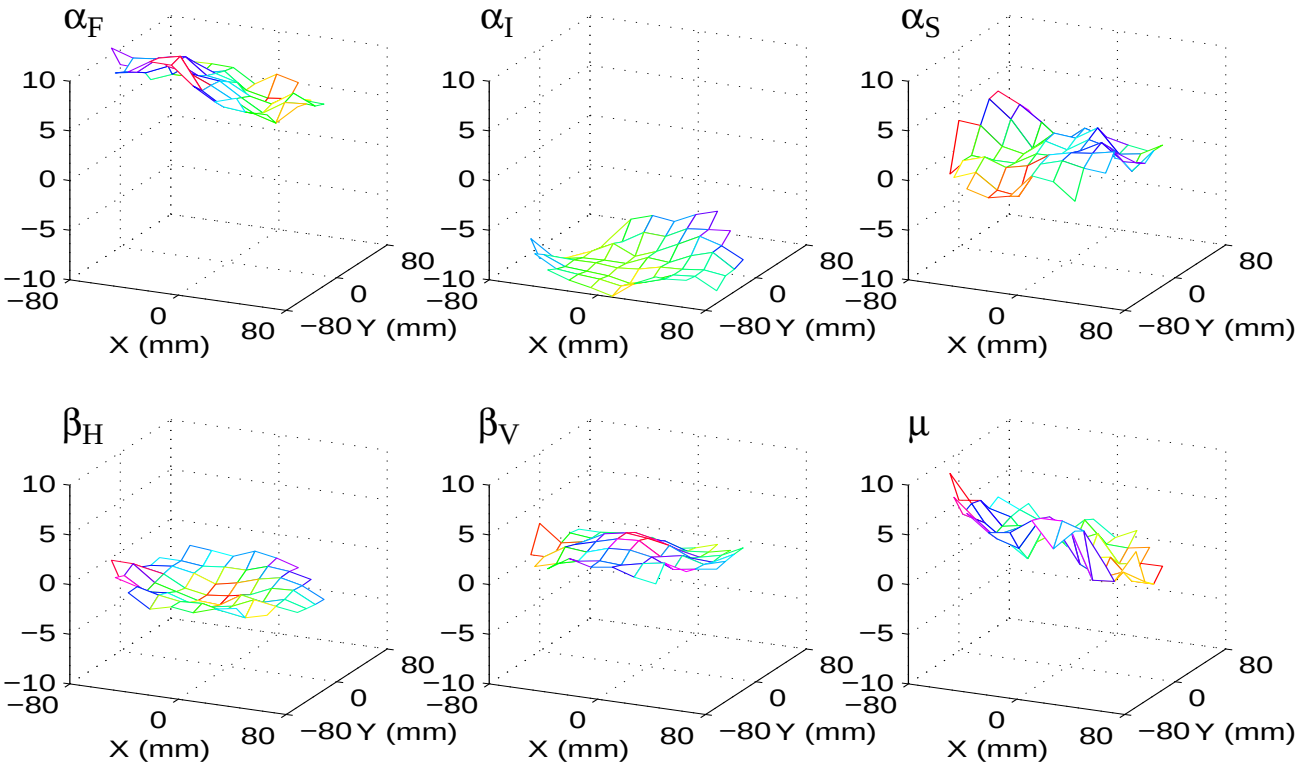


Figure 5 shows plots of the model coefficients, μ, α_F, α_I, α_S, β_H, and β_V, as a function of die spatial location on the wafer. The MANOVA procedure of the VarNOVA method described in Section 3 is used to decompose the wafer-level residuals (the difference between the raw observed variation and the extracted wafer-level variation) into die-level and wafer-die interaction components and thereby capture the majority of the systematic variation visible in Figure 4. The results of the decomposition for one particular wafer are detailed in (5) where the coefficients have been regressed onto a polynomial function of spatial position (radius from the center of the wafer, *x* position from the center of the wafer, *y* position from the center of the wafer, and the product of *x* position and *y* position from the center of the wafer.

$$\begin{bmatrix} \mu \\ \hline \alpha_F \\ \alpha_I \\ \alpha_S \\ \hline \beta_H \\ \beta_V \end{bmatrix} = \begin{bmatrix} 0.581 & -0.708 & -0.622 & 0.002 \\ \hline -0.067 & -0.548 & -0.369 & 0.085 \\ 0.355 & 0.289 & 0.275 & 0.181 \\ -0.287 & 0.259 & 0.094 & -0.266 \\ \hline 0.476 & 0.102 & -0.106 & 0.035 \\ -0.476 & -0.102 & 0.106 & -0.035 \end{bmatrix} \cdot \begin{bmatrix} r \\ x \\ y \\ x \cdot y \end{bmatrix} + \begin{bmatrix} 1.863 \\ \hline 8.470 \\ -10.410 \\ 1.941 \\ \hline -3.019 \\ 3.019 \end{bmatrix}. \quad (5)$$

As mentioned in Section 3, the terms which depend on spatial position become the wafer-die interaction components while the constant terms, i.e., those independent of spatial position, become the die-level component of the model. In this way, the die-level component of the model is common to all measured dice on the wafer. Also, the correlation coefficient for each component of the model shown in (5) is listed in Table III.

Table III. The Correlation Coefficient for the Generated VarNOVA Model

μ	α_F	α_I	α_S	β_H	β_V
0.66	0.73	0.71	0.52	0.51	-0.51

Developing a model similar to (5) serves two enabling purposes which are not easily accommodated through simpler analysis techniques. First, by developing models for all measured wafers and comparing coefficients and spatial dependencies, hypotheses regarding lot-to-lot and wafer-to-wafer variation can be tested. Furthermore, by looking at the spatial dependence of each factor type, geometric orientation versus spacing in this particular case, possible different physical and spatial dependencies can be highlighted. For example, (5) indicates that isolated features have a positive dependence on radial position while the stacked and fingered components have a negative dependence on radial position. The relatively low correlation coefficients illustrated in Table III may result from either a large random component inherent in the data and/or a more complex spatial dependence which is only properly formulated in a non-parametric sense. Nevertheless, the MANOVA model seems to capture important first-order dependencies.

5. CONCLUSION

From the methodology developed in this paper, some basic conclusions emerge from the data. The wafer-level components are about half as large in magnitude compared to the pattern dependent components (the die-level and wafer-die interaction components). This result is displayed quantitatively in Table IV.

Table IV. Wafer-Level Components Versus Pattern Dependent Components

Lot	Wafer	Range of Wafer-Level Variation (Normalized)	Range of Pattern Dependent Variation (Normalized)
A	17	24.78	46.50
A	4	18.75	43.85
B	15	20.52	38.67
B	2	25.53	40.03

For the data set analyzed in this paper, spacing, or distance to nearest structure, as well as geometric orientation are the dominant layout factors while channel width is not a significant component. However, further research is needed to understand the role of other layout factors such as poly density. Also, the role of channel width cannot be ruled out completely since only two levels are explored here and the design space for these two levels are severely unbalanced (see Table I).

Finally, the VarNOVA methodology allows simple first-order models to be developed for poly-CD variation as manifested in Id_{sat} variation. Furthermore, the models developed using this methodology allow the exploration of layout/pattern effects as a function of spatial position. The fingered structures seem to illustrate a different radial dependence compared to the isolated structures; this is an intriguing result and further research can now be targeted to explore this effect which might have otherwise been buried in noise.

The methodology presented in this paper can be extended and adapted to investigate the effect of process parameters on die-, wafer-, and wafer-die interaction components. The methodology can also be employed, using a modified experiment, to gauge the role of etch versus photolithography on polysilicon critical dimension variation.

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