Interconnects

**OUTLINE**

1. Overview of Metallization
2. Introduction to Deposition Methods
3. Interconnect Technology
4. Contact Technology
5. Refractory Metals and their Silicides

**Reading:** Plummer, Chapter 11 – Backend Technology
References: Campbell, Sections 11.9, 13.8, 15.6 - 15.10

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Interconnects

- Metal lines (within one or several layers) routed for sending signals between devices, distributing clocks, power and ground
- Metal via plugs for connecting two metal layers on different planes
- Inter Metal Dielectric (IMD) separating the metal lines
- Pads for input/output of signals
- Ohmic contact to silicon

*Fig.11.1: Schematic cross-section of backend structure, showing interconnects, contacts and vias, separated by dielectric layers (cross-hatched regions).*

**Short interconnect delays are desired i.e. minimum resistance and minimum capacitance**
Interconnect Metallization

- Six layers of Cu metallization
  - Lower layers are finer and are used for “local” interconnection between cells
  - Middle layers are wider and are used for global interconnection between blocks
  - Upper layers are wider and are used for clocks, ground and power distribution
  - Oxide is the Inter Metal Dielectric (etched)
Via Plugs
(typically Tungsten)

- Via-plugs connect layers of metal through holes in the dielectric
- Using a via-plug as contact between two layers results in planar topography
  - Eases requirements for large depth of focus (lithography)

### CMOS Drivers & Delay

\[
V_{\text{out}}(t) = \begin{cases} 
V_{\text{DD}}(1 - e^{-t_{\text{p}}/RC}) & 0 \leq t \leq t_{\text{p}} \\
V_{\text{DD}}e^{-(t - t_{\text{p}})/RC} & t \geq t_{\text{p}}
\end{cases}
\]

- \( V_{\text{DD}} \): Supply voltage
- \( t_{\text{p}} \): Propagation delay
- \( RC \): Time constant
Interconnect Metal

RC Delay

\[ R_C = \frac{\rho}{t_m} \frac{L}{W} \]

\[ C_{L} = \frac{\varepsilon_i}{t_{ox}} L W \]

\[ R_C C_L = \frac{\rho}{t_m} \frac{L}{W} \frac{\varepsilon_i}{t_{ox}} L W \]

\[ \frac{\rho}{t_m} \frac{\varepsilon_i}{t_{ox}} L^2 \]

- need low \( \rho \) to minimize RC delay
- need low \( \varepsilon_i \) to minimize RC delay
- need to increase \( t_m \) and \( t_{ox} \) to minimize RC delay

Contact / Interconnect Metallization

- Gate
- Source
- Drain
- PMOS
- NMOS

- Trench isolation
- Intermetal dielectric
- Metal 1
- Polysilicon interconnect
- Tungsten plugs
- TiN barrier
Passive Devices

- Thin Film Resistors
  - CrSi₅, Pt, TaNₓ, ZrOₓ Poly-Si
- Capacitors
  - MOS capacitors
  - Parallel plate capacitors
- Inductors
  - Spiral inductors

Examples of Inductors

What are the desirable interconnect “wiring” properties?

- Electrical
  - Low resistance
  - Low ohmic contact resistance to Si
- Physical
  - Adhesion to all surfaces
  - Good step coverage
  - Stable and reliable (corrosion and electromigration resistant)
- Process Compatibility
  - Can easily be anisotropically etched
  - Survive subsequent processing steps

Which Metal(s)?

- Al used to be the pre-dominant metal for VLSI because it meets all the requirements stated above or has a way around any problems
- Cu is now the metal for IC interconnects
Electrical Characteristics

- **Resistance**
  - Al and its alloys (Al/Cu or Al/Si) have resistivity $\rho = 3.0 \, \mu\Omega\cdot\text{cm}$ (one of the lowest)

- **Ohmic contacts**
  - Al/TiN/TiSi$_2$/n$^+$-Si or Al/TiN/TiSi$_2$/p$^+$-Si

- **Schottky contacts**
  - Al/WSi$_x$/n$^-$-Si or Al/WSi$_x$/p$^-$-Si

Physical / Mechanical Characteristics

- **Adhesion**
  - Adheres to SiO$_2$ because of chemical bonding through formation of Al$_2$O$_3$
  - Adheres to Si because of formation of Al/Si Eutectic alloy @ 577°C (can lead to spiking)

- **Step Coverage**
  - Depends on deposition process and mostly adequate
  - Surface mobility important as in CVD
  - Controlled by equipment, substrate temperature and bias

Stability and Reliability

- **Corrosion**
  - PSG + Moisture $\rightarrow$ Phosphoric acid $\rightarrow$ corrosion; **solution:** Passivation
  - Residual Cl from etching + Moisture $\rightarrow$ HCl + AlOH; **solution:** Cl removal

- **Electromigration**
  - Current flow results in voids or spike formation and circuit failure
  - High current density $\rightarrow$ e$^-$ wind $\rightarrow$ move Al along grain boundaries
  - Solution: add Cu, add high Z metals, encapsulate with oxide

Process Compatibility

- **Definition**
  - Etched in Cl-based chemistries BCl$_3$, SiCl$_4$, Cl$_2$, CCl$_4$
  - May require removal of Al$_2$O$_3$ from surface first for uniform etch
  - May require surface passivation by driving out residual Cl with F replacement (SF$_6$ plasma)

- **Subsequent Processing**
  - Al cannot withstand high temperature (660°C MT)
  - Use low temperature oxide (LTO) as inter-level dielectric (ILD)
  - Change metallization to refractory metals if high temp is absolutely necessary

PSG ≡ Phospho-Silicate Glass — SiO$_2$ doped with P$_2$O$_5$
Metal Deposition Methods

- Physical Vapor Deposition (Lecture on Wednesday)
  - Al, Al(Si), Al(Cu), Al(Si,Cu)
  - Ti, TiN, Ta, TaN
  - Cu seeding layers for electroplating

- Chemical Vapor Deposition
  - W, Ti

- Electroplating (Lecture on April 25)
  - Cu
  - Au (not used in Si VLSI)

W Chemical Vapor Deposition

**Blanket Deposition**

\[ WF_6 \text{ (vapor)} + 2H_2 \text{ (vapor)} \rightarrow W\text{(solid)} + 6HF \text{ (vapor)} \]

\[ 2WF_6 \text{ (vapor)} + 3Si \text{ (solid)} \rightarrow 2W\text{(solid)} + 3SiF_4 \text{ (vapor)} \]

**Selective Deposition** (usually two step process)

On Si surface Si reduction form \( \approx 100 \, \text{Å} \)

\[ 2WF_6 \text{ (vapor)} + 3Si \text{ (solid)} \rightarrow 2W\text{(solid)} + 3SiF_4 \text{ (vapor)} \]

In general, selective deposition occurs on nucleating surface

\[ WF_6 \text{ (vapor)} + 2H_2 \text{ (vapor)} \rightarrow W\text{(solid)} + 6HF \text{ (vapor)} \]

**Nucleating surfaces**: Si, metals, Silicides
**Non-Nucleating surfaces**: oxide, nitrides
**Cu Electroplating**

- Copper is deposited by
  - Sputtering (seeding layer for electroplating)
  - Electroplating
- Plating solutions contain Copper sulfate / Sulfuric acid
  - Many additives to control texture
- Copper is a fast diffuser in Si and it also a contaminant
  - Require a liner or diffusion barrier such as TaN

500 Å TaN
Liner/barrier layer
1000 Å sputtered Cu
Seeding layer

**Interconnect Definition**

- **Subtractive Etch**
  - Deposit metal by sputtering
  - Pattern with photoresist
  - Etch metal from areas not needed
  - Strip photoresist
- **Lift-Off**
  - Pattern photoresist
  - Deposit metal by e-beam evaporation (everywhere)
  - Dissolve photoresist to lift-off metal from field region
- **Damascene**
  - Deposit dielectric
  - Pattern photo-resist
  - Etch dielectric using PR as mask
  - Strip PR
  - Deposit Metal
  - Polish metal to be level with dielectric in field regions
**Lift-Off**

(III-V Electronic /Optoelectronic Devices)

- Chlorobenzene Assisted Lift-off
  - Pattern Photoresist
  - Soak in chlorobenzene to make the photoresist swell and form a “lip”
  - Deposit metal by e-beam evaporation
  - Dissolve photoresist to lift-off metal from field region
- Dielectric assisted lift-off (DALO) avoids chlorobenzene soak
  - Deposit dielectric which has same thickness as metal to be deposited
  - Pattern resist and etch dielectric by RIE
  - Use BOE (or isotropic over-etch) to form “lip”

**Damasene**

- Pattern photoresist
- Etch hole/trench in dielectric
- Fill holes / trenches with metal
- Etch back the metal
  - Plasma etch back
  - Chemical Mechanical Polishing

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Etch back W
**Dual Damascene**

- The dual damascene process allows the definition of the metal lines and via-plugs at the same time
  - Openings for both metal lines and via-plugs are opened in the intermetal dielectric at the same time
  - Metal for both layers are deposited at once
  - Etch back using CMP

**Planarization**

- Planar surfaces are desired
  - Depth of focus & step coverage
- Planar surface achieved by
  - Oxide reflow (BPSG)
  - Dielectric / sacrificial deposition + etch back
  - Spin-on glass (SOG)
  - Chemical Mechanical Polishing

*BPSG* = Boro-Phospho-Silicate Glass — SiO$_2$ doped with B$_2$O$_3$ and P$_2$O$_5$. It softens and re-flows at relatively low temperature because of low viscosity.
Metal-Semiconductor Contacts

- Similar to what happens at a pn junction, a metal semiconductor contact forms a junction with a barrier voltage ($\Phi_B$) and a depletion layer of width $x_d$.
- When the doping in semiconductor is low, a Schottky barrier is formed and current density $J$ is exponential with applied voltage, $V$, (like pn junction). Current is controlled by thermionic emission over the barrier.
- When the doping in the semiconductor is high, the depletion width is narrow and electrons tunnel through the barrier leading to an ohmic contact.

Ohmic Contact

- Ohmic contact resistance $\rho_C$:
  - $\rho_C = \left( \frac{3 \tau}{N} \right)^{-1}$
  - Low doping $\rho_C = \frac{kT}{qA^*T} \exp \left( \frac{\Phi_B}{kT} \right)$
  - High doping $\rho_C = \exp \left[ \frac{2\varepsilon_s}{\hbar} \left( \frac{\Phi_B}{qN_D} \right) \right]$
### Al Spiking

- **Solubility of Si in Al is high**
  - 0.5 atomic % @ 450°C
  - 1 atomic % @ 500°C
- A large amount of Si is drawn up into Al creating voids
- Voids filled by Al leading to spiking
- One solution is to use Al films that have Si in them
  - Al (1% Si)
- Another solution is to add a barrier metal between the Al and Si
  - TiSi₂ / TiN

### Refractory Metals

- Low resistivity compared to Si, poly-silicon and silicides
- Able to withstand high temperatures
- Can be deposited by CVD (conformal)
- Selective deposition into via plugs
- Excellent contact/barrier metal

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**Main applications are via-plugs, contact metallization and local interconnects**
W-Ohmic Contact

- By doping the surface of silicon heavily, very narrow depletion widths are formed at the metal / semiconductor contact
- Electrons tunnel across the very narrow barrier leading to ohmic contact
- W is excellent contact to Si
  - Able to withstand high temperatures
  - Can be deposited by CVD (conformal)
  - Selective deposition into via plugs
  - Excellent contact/barrier metal

What are Silicides?

- Formed by reaction of metal (transition or noble) with Si e.g. TiSi₂, TaSi₂, MoSi₂, CoSi₂, WSi₂, PtSi₂ etc
- Lower resistance than poly-Si. Excellent for contact, gate metal structures and thin film resistors (TFRs)
- Higher melting point than Al and hence can withstand high temperatures in back-end

<table>
<thead>
<tr>
<th>Material</th>
<th>Melting Point (°C)</th>
<th>Resistivity (µΩ-c m)</th>
<th>Thermal Expansion Coeff (10⁻⁶/°C)</th>
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<tbody>
<tr>
<td>Si</td>
<td>1420</td>
<td>500</td>
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<tr>
<td>TiSi₂</td>
<td>1540</td>
<td>13-17</td>
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<td>MoSi₂</td>
<td>1870</td>
<td>22-100</td>
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<td>41-47</td>
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<tr>
<td>W</td>
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<td>4.5</td>
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Silicide Materials Requirements

- Low resistivity
- Ease of formation
- Ease of fine line patterning
- Controlled oxidation properties
- High temperature stability
- Smooth surface features
- Corrosion resistance
- Stable contact formation to Si and Al
- Excellent Adhesion
- Low stress
- Electromigration resistance
- Low ohmic and contact resistance
- Stability during high temperature processing

Methods of Silicide Formation

- Direct Metallurgical Reaction with metal deposited by evaporation, sputter or CVD
  - \( M + x\text{Si} \rightarrow \text{MSi}_x \)
- Co-evaporation from independent Si and M source
- Co-sputtering from Independent Si and M targets
- Sputtering from a composite MSi\(_x\) target
- Chemical vapor deposition
Applications of Silicides

- Gate metallization (Polycide) — ①
- Ohmic contact / barrier metal (Salicide Technology) — ②
- Local Interconnects — ③
- Thin-Film Resistors

Polycide

Poly-Silicon / Silicide

- Formed by depositing metal on poly-silicon and reacting to form silicide + poly-silicon
  - Deposit Metal
  - Heat to form silicide
  - Etch excess metal selectively
- Used principally to reduce gate resistance of MOS devices
- Has the workfunction of poly-Silicon
- Has a reliable poly-Si/SiO₂ interface
- Can be passivated by oxidation
IC Interconnect

- Multi-layer interconnect structure
  - Al (Cu) suppresses electromigration
  - W plug in contact and vias
  - TiSi₂ contact to silicon
  - Ti/TiN promotes adhesion to oxide & suppresses electromigration

Summary

- Metals are used in
  - Interconnects (local, global, pads, power etc)
  - Contacts (Ohmic, Schottky)
  - Passives (resistors, capacitors, inductors)
- Metals deposited by
  - PVD (Sputtering and E-beam Evaporation)
  - CVD (especially W)
  - Electroplating (especially for Cu)
- Metals patterned by RIE, Damascene (Etch back & CMP), Lift-Off (GaAs only)