A 180mV FFT Processor Using Subthreshold Circuit Techniques

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Extreme Sensor Networking

Emerging Sensor Applications

Target Tracking & Detection (Courtesy of ARL)

Operating Room of the Future (courtesy John Guttag)

Machine Monitoring (courtesy ABB)

Enabler: Self-Powered Sensor System

System Power < 10\(\mu\)W for Energy Scavenging
Design Considerations

- For emerging low-performance microsensor applications, **computing speed is not critical**. Energy dissipation per function must be minimized.
- Traditional low-power design is optimized for the worst-case operating scenario.
- Significant diversity in operating scenarios:
  - Operating modes: threshold detection (low-activity), source detection (medium-activity), localization and classification (high-activity)
  - Event statistics
  - User-specified latency and quality
- The **node must be energy aware** and able to adapt energy consumption over a variety of operating scenarios.
Energy aware FFT architecture scales gracefully from 128 to 1024 point lengths and supports 8b and 16b precision.
Bit-scalable Baugh-Wooley Multiplier

- Fine-grained gating reduces activity factor and achieves energy savings with minimal area overhead.
- Bit-precision scaling architectures are used in the butterfly datapath, data memory and Twiddle ROMs.
Dedicated memory structure contains an MSB and parity-bit crossbar to avoid read/write hazards.

The energy aware control logic scales the number of butterflies with FFT length.
The optimal $V_{DD}$ for the 1024-point, 16b FFT is estimated from switching and leakage models for a 0.18µm process.

**Exploit Subthreshold Operation for Sensor Circuits**
Optimum Power Supply

There is a trade-off between leakage and switching energy as frequency, $V_{DD}$ and activity factor is varied.

The FFT design focuses on achieving supply voltages well below 400mV to investigate the minimum energy point.
Min-Max Sizing Curve

The minimum supply voltage is limited by the effect of process variations.

Inverter sizing analysis and minimum supply voltage analysis are performed at the corners.
Tiny XOR at 100mV

Leakage through the parallel devices causes the tiny XOR to fail at 100mV.
Transmission Gate XOR

- Balanced number of devices reduces the effects of leakage and process variations.
Sneak Leakage and Stacked Devices

Traditional circuits suffer from effects such as parallel leakage, stacked devices, and sneak leakage paths.

- Parallel leakage
- Sneak leakage path
- Stacked devices

A=0, B=0, C_{in} = 0

idle current

drive current
Buffering, reducing parallel devices, and driving device gates are methods used in subthreshold standard cell logic design.
Sizing Tradeoffs - SRAM cell

Increasing $W_{N2}$ prevents the memory cell from being rewritten during a read access.

Write condition trade-off

$W_{N3}/W_{P1}$ large: write ‘0’ into HI at the SF corner
$W_{N2}/W_{P2}$ small: write ‘1’ into LO at the FS corner
Tristate latch-based write access achieves low voltage operation at process corners.
Read Bitline at 100mV

Data dependent leakage
Worst case output-high: 
M₀=0, M₁-M₁₂₇=1
Worst case output-low: 
M₀=1, M₁-M₁₂₇=0
The hierarchical-read bitline eliminates parallel leakage and stacked devices.
Latch-Write and Hierarchical-Read Memory

- Muxes are daisy-chained for compact layout area.
Custom Subthreshold FFT

Process Details
- 0.18µm CMOS process
- 6 layer metal
- 628k transistors

Design Flow
- Custom subthreshold logic cells
- Custom Skill-based memory generators and multipliers
- Skill code place-and-route
The FFT processor achieves 180mV operation for 16-bit, 1024-point operation. The clock frequency is 164 Hz.

180 mV Supply Demonstration

- The FFT processor achieves 180mV operation for 16-bit, 1024-point operation. The clock frequency is 164 Hz.
The FFT is able to operate at 128, 256, 512 and 1024-point FFT lengths and 8 and 16b precisions.

8b processing leads operation at a larger minimum $V_{DD}$ due to reduced activity factor.
Energy Estimation

- The FFT operates between $V_{DD}=180\text{mV}-900\text{mV}$ and clock frequency of $164\text{Hz}-6\text{MHz}$.
- The minimum energy dissipated is $155\text{nJ/FFT}$ at $350\text{mV}$ for a 1024-point 16b FFT. The clock frequency is $10\text{kHz}$ and the FFT processor dissipates $0.6\mu\text{W}$. 
Conclusions

- Subthreshold operation at the optimal supply voltage and clock frequency is necessary to minimize energy dissipation of digital circuits in wireless sensor applications.
- Process variations limit the minimum supply voltage operation of CMOS circuits.
- Subthreshold logic and memory design methodology minimizes parallel leakage, stacked devices and sneak leakage effects.
- Demonstrated a 180mV FFT Processor using subthreshold circuit techniques.