Substrate Noise Analysis and Experimental Verification for the Efficient Noise Prediction of a Digital PLL

Nisha Checka, Anantha Chandrakasan, Rafael Reif

Microsystems Technology Laboratory, MIT
60 Vassar St. Rm. 39-625
Cambridge, MA, (USA) 02139
Outline

- Background
- Conventional substrate noise simulation
- Noise macromodels
- Substrate Noise Analysis Tool (SNAT)
  - Overview
  - Measurement comparison
- Summary
Background: Noise Generation

- Digital circuits inject noise into substrate during high speed switching
- Noise Sources:
  - Vdd/gnd bounce
  - Switching inputs/outputs
  - Bulk current
Background: Noise Generation

- Noise travels to analog section via conductive substrate
- Effect on analog circuits: power/gnd noise, pick-up through depletion capacitances, vary bias through $V_T$ fluctuation, backgate effect
Motivation

- UWB transceiver chip
  - TSMC 0.18 μm mixed mode process

*Figures courtesy F. Lee*
Model needs to be simplified to yield reasonable simulation times

Solution: Extract noise behavior into equivalent macromodel
Noise Macromodel Derivation

- Represent each noise source with equivalent source in macromodel
  - Represent $V_{dd}/gnd$ bounce with $I_{VDD}$ and $I_{VSS}$ and $Z_{VDD}$ and $Z_{GND}$
  - Represent switching inputs/outputs with $V_{sw}$ and $Z_{INT}$
  - Represent bulk current with $I_{BULK}$

- $C_D$ represents circuit decoupling capacitance

Based on (Badaroglu et.al., JSSC vol.37, no.11)
Substrate Noise Analysis Tool

- **Inputs**
  - Circuit description: netlist or gate level description
  - Technology information: as detailed as substrate doping profiles, as coarse as substrate resistivity and type

- **Outputs:**
  - Time domain substrate noise
  - Noise spectrum
Granularity Level

- **Inputs: Circuit Description**

<table>
<thead>
<tr>
<th>Short Run Time</th>
<th>Increasing Accuracy</th>
<th>Long Run Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Least Descriptive</td>
<td></td>
<td>Most Descriptive</td>
</tr>
</tbody>
</table>

  - Gate level netlist
  - SPICE netlist
  - SPICE netlist w/ parasitics

  ```
  module adder(A,B,Cin,S,Cout);
  input A, B, Cin;  output S, Cout;
  assign S = A ^ B ^ Cin;
  assign Cout = (A & B) | (A & Cin) | (B & Cin);
  endmodule
  ```

- **Inputs: Technology Description**

<table>
<thead>
<tr>
<th>Short Run Time</th>
<th>Increasing Accuracy</th>
<th>Long Run Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Least Descriptive</td>
<td></td>
<td>Most Descriptive</td>
</tr>
</tbody>
</table>

  - Substrate resistivity (no layout information)
  - Substrate resistivity (w/ contacts layout)
  - Substrate doping profile (full layout)
Measurement Comparison

- Test circuit: Digital PLL (~ 15K gates)
  - Designed in TI’s 90nm technology
  - $f_{\text{clkref}} = 80$ MHz, $f_{\text{out}} = 480$ MHz
  - Substrate noise sensors added around DPLL
Granularity Levels

- **Inputs: Circuit Description**
  - Short Run Time (Least Descriptive)
  - Increasing Accuracy
  - SPICE netlist (Nanosim level 2)
  - SPICE netlist (Nanosim level 1)
  - SPICE netlist w/ parasitics (Nanosim level 1)
  - Mimic gate level netlist

- **Inputs: Technology Description**
  - Short Run Time (Least Descriptive)
  - Increasing Accuracy
  - Substrate resistivity (no layout)
  - Substrate resistivity (w/ contacts layout)
  - Substrate doping profile (full layout)
  - SNAT generated
  - SNAT generated
  - SubstrateStorm
Noise Spectrum

- Top sensor
- SNAT Simulation:
  - Technology Description: SubstrateStorm generated model
    - ~ 30 minutes to generate netlist
    - ~ 51 hours to simulate
  - Circuit Description: SPICE netlist (no parasitics)
    - ~ 6 minutes

Comparison of Measurements and SNAT Simulation

![Graph showing comparison of measurements and SNAT simulation](image)
Error

- Most error at 80 MHz ($f_{\text{clkref}}$) and 480 MHz ($f_{\text{out}}$)
Parasitics

- Incorporate effect of pad parasitics – REFCLK pad and CLKOUT pad
  - Pad to substrate capacitance
  - Capacitance to substrate of ESD structures
- Highest accuracy level – 11.7% error in RMS voltage

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>11.7%</td>
</tr>
<tr>
<td>500</td>
<td>0%</td>
</tr>
<tr>
<td>1000</td>
<td>0%</td>
</tr>
</tbody>
</table>

![Sensor 1 - Percent Error from Measurements](image_url)
**Noise Spectrum**

- **Top sensor**
- **SNAT Simulation:**
  - Technology Description: SubstrateStorm generated model
    - ~30 minutes to generate netlist
    - ~51 hours to simulate
  - Circuit Description: SPICE netlist with parasitics
    - ~6 minutes

*Comparison of Measurements and SNAT Simulation*

> 11.7% error in RMS voltage
Effect of Substrate Model
Granularity Levels

- Inputs: Circuit Description
  - Short Run Time
    - Least Descriptive
  - Increasing Accuracy
  - SPICE netlist (Nanosim level 2)
  - Mimic gate level netlist
  - Long Run Time
    - Most Descriptive

- Inputs: Technology Description
  - Short Run Time
    - Least Descriptive
  - Increasing Accuracy
  - Substrate resistivity (no layout)
    - SNAT generated
  - Substrate resistivity (w/ contacts layout)
    - SNAT generated
  - Long Run Time
    - Most Descriptive
  - Substrate doping profile (full layout)
    - SubstrateStorm
Substrate Model

Substrate Transfer Functions

Gain (dB)

Frequency (MHz)
Substrate Model

- SNAT does not consider capacitive effects of wells and junctions
  - Treats substrate as purely resistive
- Parasitics included
- SNAT-generated substrate model (<15 mins) vs. SubstrateStorm-generated model (51+ hrs)

---

**Percent Error from Measurements (Different Substrate Models)**

![Graph showing error vs. frequency for different substrate models.](image-url)
Substrate Model

- SNAT does not consider capacitive effects of wells and junctions
  - Treats substrate as purely resistive
Error

- Parasitics included
- SNAT-generated substrate model (<15 mins) vs. SubstrateStorm-generated model (51+ hrs)
Time Domain – Effect of Substrate Model

Simulated Substrate Noise Voltage (Different Substrate Models)

- Time (ns)
- Voltage (mV)

lev8
lev10
Substrate Model

- SNAT does not consider capacitive effects of wells and junctions
  - Treats substrate as purely resistive
Substrate Model

- SNAT does not consider capacitive effects of wells and junctions
  - Treats substrate as purely resistive
Error

- Parasitics included
- Substrate models:
  - SNAT + no layout substrate model (<10 seconds)
  - SNAT + layout substrate model (<15 mins)
  - SubstrateStorm generated model (51+ hrs)

Percent Error from Measurements (Different Substrate Models)

455% error
Measurement Comparison

- Test circuit: Digital PLL (~ 15K gates)
  - Designed in TI’s 90nm technology
  - $f_{\text{clkref}} = 80$ MHz, $f_{\text{out}} = 480$ MHz
  - Substrate noise sensors added around DPLL
Right Sensor

- Substrate transfer function varies with sensor location
Summary

- Substrate Noise Analysis Tool (SNAT)
  - Works at any point in design cycle
  - Measured substrate noise performance of the TI DPLL
    - 11.7% error in RMS voltage
  - Can achieve a dramatic speed-up in run-time with a doubling in the error
  - Coarsest macromodel simulation can get used to yield noise order of magnitude estimate in minutes
Acknowledgements

- MARCO Interconnect Focus Center
- Texas Instruments, Inc.
  - Fellowship support
  - Neeraj Nayak, Mohamed Mahmoud, Chris Barr, Baher Haroun
Macromodel Simulation

Original circuit

Equivalent Macromodel
Example

- Granularity level
  - Circuit: gate level netlist

Example: One bit adder

Replace each cell with equivalent macromodel
Noise Simulation

- Represent each digital block with equivalent macromodel
- Construct macromodel for entire chip

Sample macromodel for entire digital system (assuming epi substrate)