An Energy Efficient OOK Transceiver for Wireless Sensor Networks

Denis C. Daly and Anantha P. Chandrakasan

Microsystems Technology Laboratories,
Massachusetts Institute of Technology
Cambridge, MA 02139, USA

***Abstract*— A 1 Mbps 916.5 MHz OOK transceiver for wireless sensor networks has been designed in a 0.18-μm CMOS process. The RX has an envelope detection based architecture with a highly scalable RF front end. The RX power consumption scales from 0.5 mW to 2.6 mW, with an associated sensitivity of -37 dBm to -65 dBm at a BER of 10^{-3}. The TX consumes 3.8 mW to 9.1 mW with output power from -11.4 dBm to -2.2 dBm. The RX achieves a startup time of 2.5 μs, allowing for efficient duty cycling.**

***Index Terms*— energy efficient, low power, sensor networks, transceivers.**

I. Introduction

A microsensor network consists of a group of sensor nodes that are deployed remotely and used to relay sensing data to the end-user. Applications for sensor networks range from military, such as target tracking, to consumer electronics and industrial equipment, such as home lighting or distributed sensing of factory equipment. As sensor networks mature, it is expected that nodes will reduce in size and cost, allowing for the emergence of large scale sensor networks consisting of thousands to millions of nodes [1].

A key metric for measuring the energy efficiency of wireless transceivers is *energy per bit*, representing the average amount of energy required by a transceiver to transmit or receive a single bit of data. Previously published low-power, short range radios have achieved an energy per bit as low as 10 nJ/bit [2], [3].

This paper presents a 0.18-μm CMOS wireless transceiver suitable for large scale sensor networks with closely spaced nodes ($<$10 m apart). Through the use of high data rates and a scalable architecture, this transceiver achieves energy per bit ratios as low as 0.5 nJ/bit for the receiver and 3.8 nJ/bit for the transmitter. The receiver has a startup time of 2.5 μs, allowing for efficient duty cycling. Due to the transceiver's scalability, energy efficiency can be maximized over a wide range of operating conditions.

II. Architecture and System Specifications

A block diagram of the transceiver is shown in Fig. 1. The transceiver operates in a single channel centered at 916.5 MHz and employs on-off keying (OOK) modulation. The receiver uses an envelope detection based architecture that eliminates the need for a local oscillator. The transmitter generates the OOK waveform by modulating the output of a surface acoustic wave (SAW) stabilized oscillator. Both the transmitter and receiver are designed to maximize energy efficiency. Passive SAW components allow for reduced power consumption and die area at the expense of reduced integration and flexibility. Motivations for these system and architectural specifications are described in the following subsections.

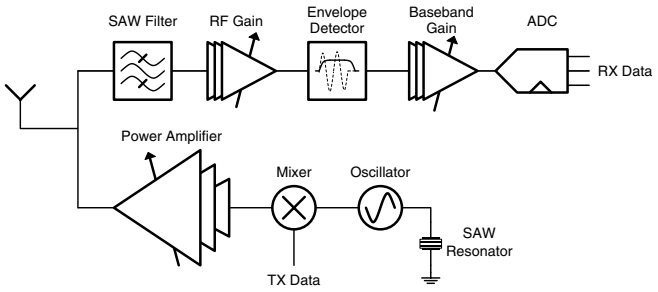


Fig. 1. Architecture of proposed transceiver

A. Modulation

Traditional cellular systems place a high value on spectral efficiency and thus use efficient modulation schemes like differential quadrature phase-shift keying (DQPSK). A drawback to these modulation schemes is that they typically result in greater transceiver power consumption than less spectrally efficient modulation schemes like OOK [4]. OOK is well suited for energy efficient short-range wireless links where transceiver power consumption is often greater than power amplifier (PA) output power. A non-coherent, OOK receiver is proposed to enable the use of an envelope detection based receiver. By using a non-coherent receiver instead of a coherent receiver, no oscillator is required for phase synchronization and the receiver can turn on quickly.

B. Data Rate

For sensor network applications like acoustic tracking and detection, a data rate of only hundreds to thousands of bits per second is required. However, for optimal energy efficiency it is often advantageous to operate the transceiver at a higher instantaneous data rate and turn off the radio periodically.

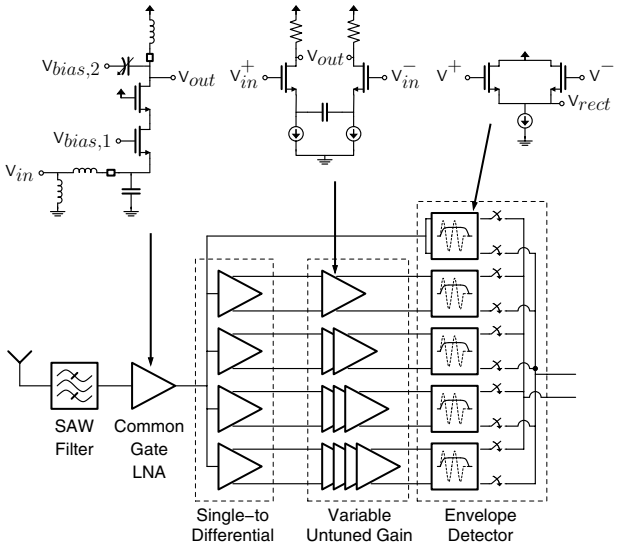


Fig. 2. Receiver front end

The transceiver operates at a data rate of 1 Mbps, which allows many nodes to share the same channel through time division multiplexing. A continuous-time envelope detector architecture is used instead of super-regenerative sampling to avoid the need for precise control of a quench signal [5].

III. Transceiver Implementation

A. Receiver Front End

A detailed block diagram of the receiver front end is shown in Fig. 2. A common-gate low noise amplifier (LNA) with a tuned LC load first amplifies the radio-frequency (RF) input. The load capacitor is implemented as an accumulation mode on-chip capacitor to allow for tuning and the load inductor is off-chip. Following the LNA are 5 separate slices, each corresponding to a different gain setting. The RF front end startup time is less than a microsecond as it is set by the settling time of bias currents.

To support gain scalability and achieve optimal energy efficiency over a wide range of operating conditions the front end has multiple gain settings. A sequential gain architecture is used, in which a variable number of gain stages can be activated at any time [6]. At any given time, only 1 horizontal slice is active. At the lowest gain setting, the LNA output is directly fed to the envelope detector, whereas at the highest gain setting, the LNA output is amplified by 5 resistively loaded RF amplifiers. The first amplifier in each slice acts as a single-to-differential converter. Later amplifiers are differential amplifiers with capacitively coupled source terminals. This circuit topology serves to mitigate the effect of cascaded dc offsets while allowing for good high-frequency common-mode rejection.

Parallel slices are used instead of a single slice with multiple output taps to allow for each gain setting to have different device sizing and bias currents. To meet noise constraints at high gain settings, the single-to-differential converter load resistors are decreased and bias currents are increased from their optimal power efficiency values. The area overhead of these parallel slices is minimal, due to the small size required by each untuned amplifier. The motivation for and optimization of these untuned amplifiers is outlined in the following section.

B. Energy Efficient RF Gain

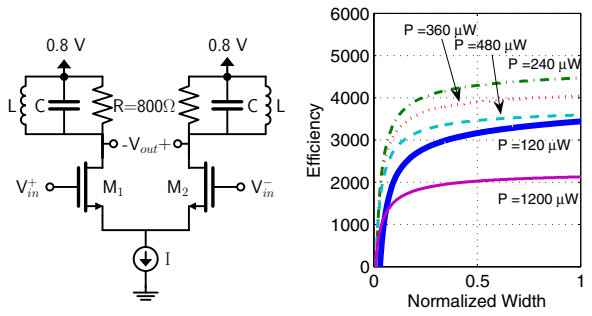
For the receiver envelope detector to properly function, the RF input must be amplified to approximately 60 $\mathrm{mV_{PP}}$. Given an input signal of -65 dBm, a voltage gain of 45 dB is required. Even if it were possible to achieve such a large gain in a single stage, it would not necessarily be the most energy efficient approach. In [7], Meindl and Hudson derive the optimal number of stages for BJT and CMOS amplifiers in a variety of configurations to minimize power consumption. Their approach serves as the basis for the following general energy efficiency metric:

$$E = f(Gain, Power) = \frac{log(Gain)}{Power} \tag{1}$$

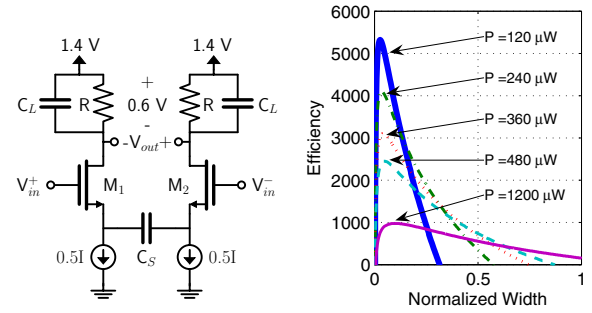
This metric can be intuitively explained by noting that for cascaded, identical gain stages, the total gain increases exponentially with the number of stages whereas power consumption increases linearly.

The metric described in Equation 1 is used to determine the optimal amplifier topology as well as appropriate biasing and sizing of devices. In particular, the efficiency of a tuned amplifier is compared to an untuned, resistively loaded RF amplifier as shown in Fig. 3. For the tuned gain circuit, the resonant load is assumed to have an impedance of 800 Ω, corresponding to a tank quality factor of approximately 28 for typical tank configurations. For the untuned gain circuit, a voltage drop of 0.6 V across the load resistors is assumed. To accurately model the capacitive loading at the output of the untuned gain stage, identical untuned gain stages are cascaded. For both topologies, the bias current, I, is swept over multiple values and the width of the input transistors is also varied.

Fig. 3 presents the corresponding energy efficiency of the tuned and untuned gain stages. We see that at 915 MHz in the given 0.18-μm CMOS process, the maximum energy efficiency of an untuned, resistively loaded differential pair is superior to that of a tuned differential pair by approximately 20%. This conclusion motivates the RF front end architecture shown in Fig. 2. The first amplifier is a tuned LNA to improve noise-performance of the receiver, but later stages are all untuned amplifiers to maximize energy efficiency. Untuned amplifiers have the additional benefit of not occupying significant die area, thereby reducing the cost and size of the sensor node.



(a)



(b)

Fig. 3. Efficiency of (a) tuned and (b) untuned RF gain versus normalized input transistor width. Transistor-level schematics of the tuned and untuned RF gain stages are shown to the left of the efficiency curves.

C. Baseband Amplifier and ADC

The envelope detector operates similarly to a diode-based rectifier and is a differential pair with the output at the source node of the input pair. Fig. 4 presents a measured plot of antenna input amplitude versus envelope detector output amplitude for each of the 5 gain settings. For correct operation the pseudo-differential envelope detector output must have an amplitude greater than approximately 5 mV_{PP}, corresponding to the dotted horizontal line in Fig. 4. At lower amplitudes, thermal noise and kickback from the analog-to-digital converter (ADC) introduce bit errors. The baseband amplifier consists of 3 resistively loaded amplifiers, each with input-mode offset compensation. The offset compensation includes preset switches to reduce the settling time at startup. Later stages of the baseband amplifier can be disabled to reduce the overall gain. Given the extensive scalability preceding the ADC and the simplicity of OOK modulation, the 8 MSPS ADC needs only 3 bits of resolution.

D. Transmitter

The transmitter schematic is shown in Fig. 5. The transmitter generates a 1 Mbps Manchester encoded OOK signal.

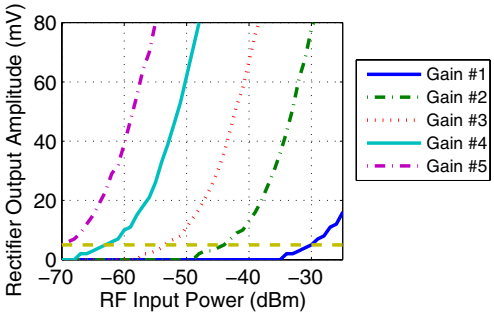


Fig. 4. Envelope detector output amplitude versus RF input power

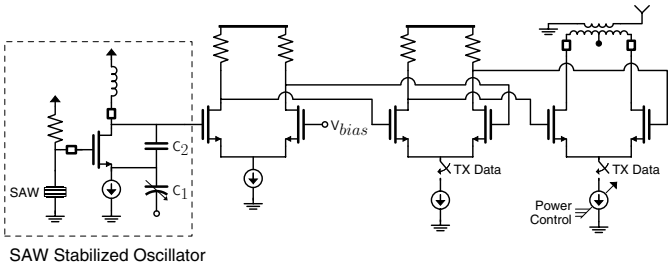


Fig. 5. Transmitter schematic

Although the transceiver can support other types of modulation, Manchester encoding is used to simplify the off-chip baseband demodulator. The SAW stabilized oscillator consists of a Colpitts oscillator coupled to a SAW resonator. The startup time of the oscillator is set by the SAW resonator and is measured to be less than 60μs. Since the oscillator startup time is longer than a bit period, it cannot be power gated when transmitting a '0'.

The mixer is integrated with the PA, which consists of 2 cascaded untuned differential pairs followed by a tuned amplifier. The first 2 PA stages buffer the single-ended oscillator output and convert it to a differential signal. The differential signal allows for a 500 ns OOK pulse width with minimal switching transients. When transmitting a '0', the final two stages of the PA are disabled to reduce power consumption. The final amplifier is loaded with an off-chip balun to generate a single-ended output while attenuating harmonic distortion. The PA power output is adjustable through digital control of the final amplifier's bias current.

IV. Measured Results

The receiver power consumption scales from 0.5 mW at the lowest gain setting to 2.6 mW at the highest gain setting. The receiver achieves a maximum sensitivity of -65 dBm at a bit error rate (BER) of 10^{-3}. Fig. 6 presents the measured BER of the receiver versus input power for each of the five RF gain settings. The startup time of the receiver is 2.5 μs, significantly faster than most PLL based receivers.

The transmitter supports 7 output power levels from

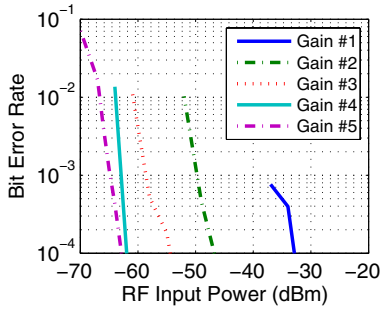
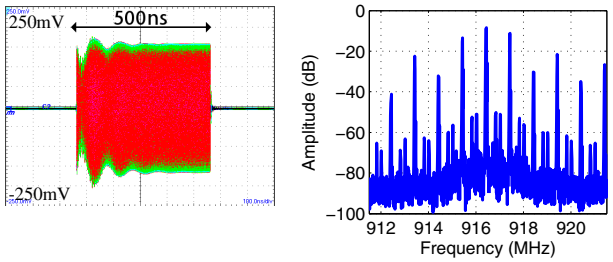


Fig. 6. Bit error rate versus input power for each RF gain setting



(a) (b)

Fig. 7. Power amplifier (a) envelope and (b) frequency spectrum

-11.4 dBm to -2.2 dBm and achieves a peak efficiency of 6.9%. The oscillator achieves a phase noise of -114.3 dBc/Hz at a 1 MHz offset from the carrier. Fig. 7 presents the envelope and frequency spectrum of the PA output when transmitting a Manchester encoded sequence of '1's.

Fig. 8 presents a chip micrograph of the transceiver. The active area of the chip is 0.27 mm^2, however the die area is 1.3 mm by 1.4 mm as the chip is pad limited. The radio has been integrated and tested on an acoustic sensor board that includes a microphone, ADC and DSP. A summary of results are presented in Table I.

V. Conclusions

A 1 Mbps energy efficient transceiver for wireless sensor networks has been demonstrated. The transceiver is highly scalable and achieves a fast receiver startup time, which allows for efficient operation in low duty cycle, energy starved scenarios. The transceiver architecture lends itself well to process and voltage scaling due to the absence of op amps and precise feedback loops. The radio achieves an energy-per-bit ratio as low as 0.5 nJ/bit for the receiver and 3.8 nJ/bit for the transmitter.

Acknowledgment

We thank National Semiconductor for chip fabrication and Peter Holloway for his support and feedback. This work is sponsored by Defense Advanced Research Projects Agency (DARPA) and Air Force Research Laboratory, under agreement number F33615-02-2-4005.

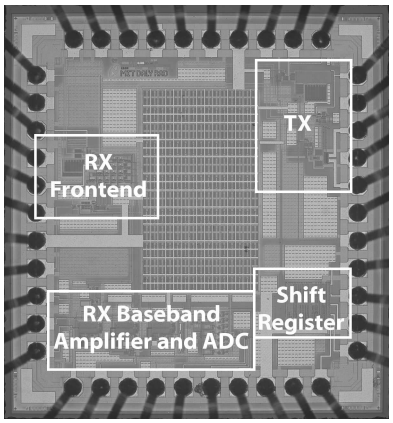


Fig. 8. Chip micrograph of the transceiver in 0.18-μm CMOS

TABLE I
Performance Summary

System Specifications	
Data Rate	1 Mbps
Center Frequency	916.5 MHz
Technology	0.18-μm CMOS
Die Area	1.3 mm by 1.4 mm
Receiver (5 gain settings)	
Power Consumption	2.5 to 0.5 mW
Sensitivity at 10^{-3} BER	-65 to -37 dBm
Startup Time	2.5μs
Transmitter (7 power settings)	
Power Consumption	3.8 to 9.1 mW
Output Power	-11.4 to -2.2 dBm
Startup Time	$<$60μs

References

[1] J. M. Kahn, R. H. Katz, and K. S. J. Pister, "Next Century Challenges: Mobile Networking for "Smart Dust"," in *International Conference on Mobile Computing and Networking (MOBICOM)*, Seattle, WA, Aug. 1999, pp. 271–278.

[2] A. Vouilloz, M. Declercq, and C. Dehollain, "A Low-Power CMOS Super-Regenerative Receiver at 1 GHz," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 2186–2196, Dec. 2001.

[3] S. Cho and A. P. Chandrakasan, "A 6.5 GHz CMOS FSK Modulator for Wireless Sensor Applications," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 2002, pp. 182–185.

[4] A. Wang, S.-H. Cho, C. Sodini, and A. Chandrakasan, "Energy Efficient Modulation and MAC for Asymmetric RF Microsensor Systems," in *IEEE International Symposium on Low Power Electronics and Design*, Aug. 2001, pp. 106–111.

[5] B. Otis, Y. Chee, and J. Rabaey, "A 400μW-RX 1.6mW-TX Super-Regenerative Transceiver for Wireless Sensor Networks," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2005, pp. 396–297, 606.

[6] M. Gehring, R. Moen, L. Ragan, and D. Ash, "A Sequential-Gain IC for Miniature Short-Range Battery-Powered Wireless Data Receivers," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 1995, pp. 142–143.

[7] J. D. Meindl and P. H. Hudson, "Low Power Linear Circuits," *IEEE Journal of Solid-State Circuits*, vol. 1, pp. 100–111, Dec. 1966.