An Energy Efficient Sub-Threshold Baseband Processor Architecture for Pulsed Ultra-wideband Communications

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ICASSP – Toulouse May 14 – 19, 2006
■ UWB Specifications and System Architecture
■ Baseband Algorithm and Architecture
■ Parallelism for Energy Efficiency
  □ Mapping of Algorithm → Minimize System Energy
  □ Circuit Optimization → Minimize Baseband Energy
■ Challenges for Highly Parallelized Designs
■ Conclusions
Ultra-wideband (UWB) Radio

Advantages of UWB communications include
- High Data Rate
- Excellent Multipath Resolution
- Low Interference

Integrate UWB radios on battery operated devices

Need an energy efficient UWB System
UWB System Architecture

![14 Channel Frequency Plan](image.png)

- **Frequency [GHz]**: 3.1, 10.6
- **Power density [dBm]**: -41.3, -51.3, -61.3

**Figure courtesy of D. Wentzloff**

![Digital Baseband Processor](image.png)

**Sampling Rate**: 500 MSPS
Packet Structure

- **Goal**: Reduce overhead energy (PREAMBLE)

- **PREAMBLE**
  - 31-bits
  - 40ns

- **PAYLOAD**
  - 10ns

- **States**:
  - **State 0**: Acquisition
  - **State 1**: Channel Estimation
  - **State 2**: Payload Detection
  - **State 3**: Demodulation

- **Receiver**
  - Turns ON
  - Turns OFF
Baseband Algorithm

- Acquisition Phase
  - Detect packet
  - Estimate delay
  - Synchronize

- Channel Estimation
  - Measure multipath in wireless channel

- Payload Detection
  - Wait for inverted replication

- Demodulation
  - Adjust for multipath
  - Resolve bit
Baseband Architecture

- Majority of preamble energy spent on computation of cross-correlation
- Fixed number of operations
- Map operations to architecture that reduces system energy
- Reduce energy of each operation
Exploit **TWO** forms of parallelism in Correlator Bank

- **Mapping of Algorithm: Parallelized Computation (M)**
  - Reduce acquisition time
  - Minimize System Energy (Energy per packet)

- **Circuit Optimization: Maintain Throughput (L)**
  - Reduce supply voltage
  - Minimize Baseband Energy (Energy per operation)
System Energy Savings (Mapping)

- Trade-off area for time by mapping to parallel architecture
- Reducing acquisition time allows for fewer number of Gold Code repetitions in the preamble
- RF front-end and ADC can be turned off earlier
- **Energy savings across the entire system**
  - Reduce energy per packet

![Graph showing energy savings across parallelism](chart.png)
Preamble Energy Reduction

Reduce RF front-end and ADC energy!

14X overall reduction

Digital Baseband  ADCs  Baseband Amplifiers  RF front end

Parallelism (M)

Preamble Energy (normalized)

1.2  1.0  0.8  0.6  0.4  0.2  0.0

1  4  8  11  16  31

14X overall reduction
Energy Reduction vs. Payload Size

Payload Percentage

Payload Energy Dominates

Preamble Energy Dominates

Energy Reduction (%) for M=31 vs. M=1

Payload Size (bytes)
Correlators compute the cross-correlation function

- Fixed number of operations required
- Voltage scale to reduce energy per operation
- Parallelize to maintain throughput of 500 MSPS
- Designed and simulated in a 90-nm process (STMicroelectronics)
Selection of Optimum Supply Voltage

![Graph showing the relationship between supply voltage and energy per operation](image-url)

- **Supply Voltage $V_{DD}$ (V)**
- **Energy per operation (normalized)**

Minimum Energy Point

- Supply Voltage $V_{DD}$ (V) at the minimum energy point.
Minimum Energy Point

\[ E_{\text{dynamic}} \propto C_{\text{eff}} V_{DD}^2 \]

\[ E_{\text{leakage}} \propto T_{\text{period}} V_{DD} I_{\text{leak}} \]

\[ E_{\text{total}} = E_{\text{dynamic}} + E_{\text{leakage}} \]

Characteristic of typical NMOS device

Strong Inversion \((V_{DD} > V_T)\)

\[ T_{\text{period}} \propto \frac{V_{DD}}{(V_{DD} - V_T)^2} \]

Sub-Threshold \((V_{DD} < V_T)\)

\[ T_{\text{period}} \propto \frac{V_{DD}}{(V_{DD} - V_T) e^{nkT/q}} \]

for \(V_{GS} = V_{DD}\)
Correlator Energy per Operation

![Diagram showing energy per operation as a function of supply voltage. The graph labels include 'Minimum Energy Point', 'Total Energy', 'Dynamic Energy', and 'Leakage Energy'. The y-axis represents energy per operation (normalized) on a logarithmic scale, while the x-axis represents supply voltage \( V_{DD} \) (V).]
Baseband Energy Savings

- At the minimum energy point of 0.3 V
  \[ \rightarrow \text{reduce energy per operation by 9X} \]
- Set clock frequency to 25 MHz (preamble PRF)
- Parallelize by L=20 to maintain 500 MSPS throughput
- Need to raise voltage to 0.4 V to achieve 25 MHz
- At 0.4 V, \text{reduce energy per operation by 5.8X}

Minimum energy when baseband operates in sub-threshold
Parallelized Baseband Architecture

5-bit Input from ADC

5 Tap FIR Filter

Correlator Bank

Correlator Sub-bank 1
- Correlator 1
- Correlator 2
- ... (L correlators)

Correlator Sub-bank 2
- Correlator L+1
- Correlator L+2
- ... (L correlators)

Correlator Sub-bank M
- Correlator (M-1)L+1
- Correlator (M-1)L+2
- ... (L correlators)

Threshold Detector/Position Encoder

FIR Coefficients

Demodulation

5 Tap FIR Filter

5 Tap FIR Filter

5 Tap FIR Filter

5 Tap FIR Filter

Demodulated Bits

Bit Decoder

L = 20

M = 31

Total # of correlators = 620
Challenges with High Parallelism

- Major concerns for highly parallelized designs
  - Increased Leakage Current
  - Increased Interconnect Capacitance

- Use **power gating** to reduce leakage current

- Use **clock gating and careful layout** to reduce switching interconnect capacitance
- Larger number of transistors result in larger leakage currents
- Reduce leakage power by using a transistor to gate the leakage current when block is idle
Conclusions

- Reduce energy to receive a UWB packet by
  - Mapping algorithm to parallel architecture
  - Scaling to optimum supply voltage

- Reduced acquisition time
  - 14X reduction in preamble energy
  - 43% energy reduction for a 500 byte packet

- Voltage scaling to sub-threshold (1 V → 0.4 V)
  - 5.8X reduction in energy per operation of correlators

- This analysis can be applied to other high performance communication applications