An Energy Efficient Sub-Threshold Baseband Processor Architecture for Pulsed Ultra-wideband Communications

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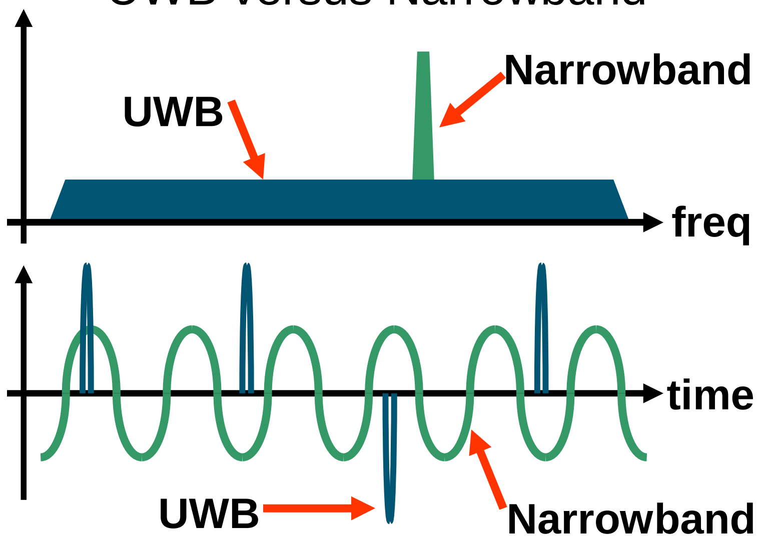
Outline

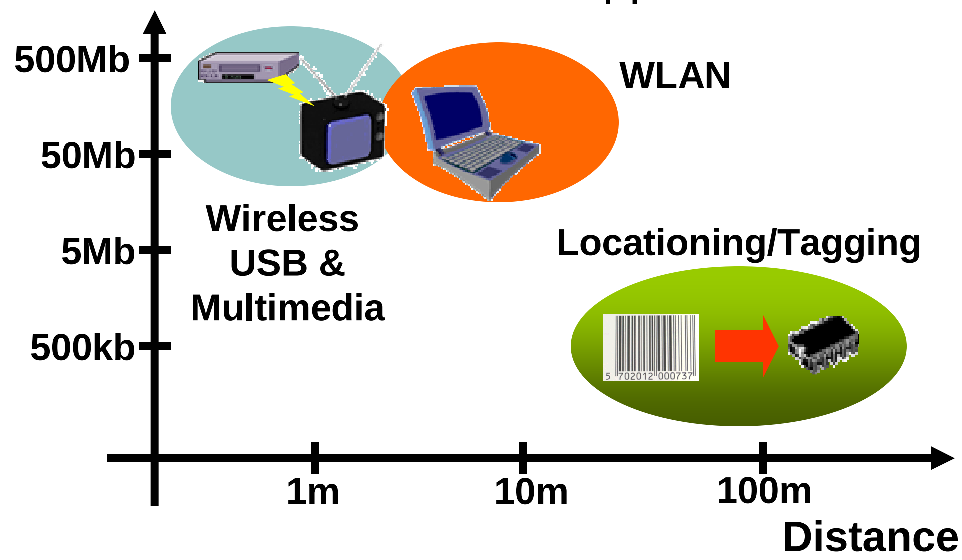
- UWB Specifications and System Architecture
- Baseband Algorithm and Architecture
- Parallelism for Energy Efficiency
  - Mapping of Algorithm → Minimize System Energy
  - Circuit Optimization → Minimize Baseband Energy
- Challenges for Highly Parallelized Designs
- Conclusions

Ultra-wideband (UWB) Radio

UWB versus Narrowband

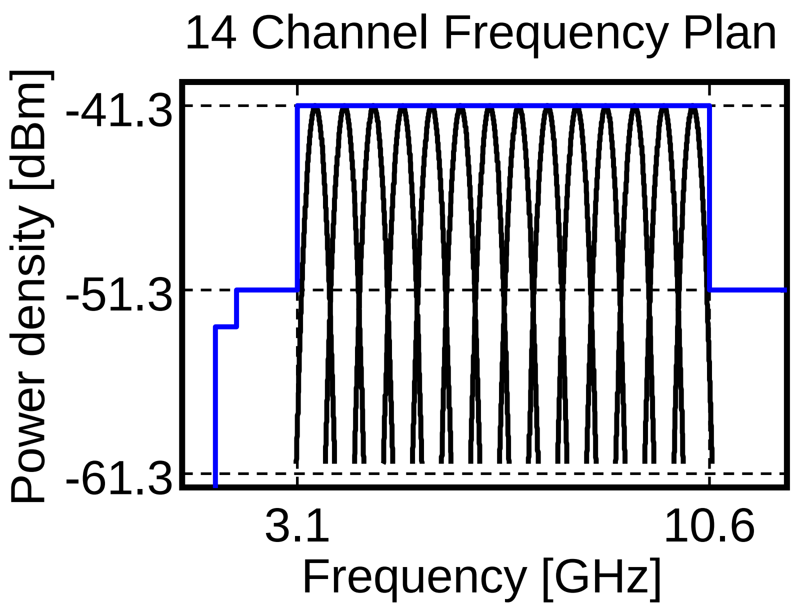


Possible UWB Applications



- **Advantages of UWB communications include**
  - **High Data Rate**
  - **Excellent Multipath Resolution**
  - **Low Interference**
- **Integrate UWB radios on battery operated devices**
- **<u>Need an energy efficient UWB System</u>**

UWB System Architecture



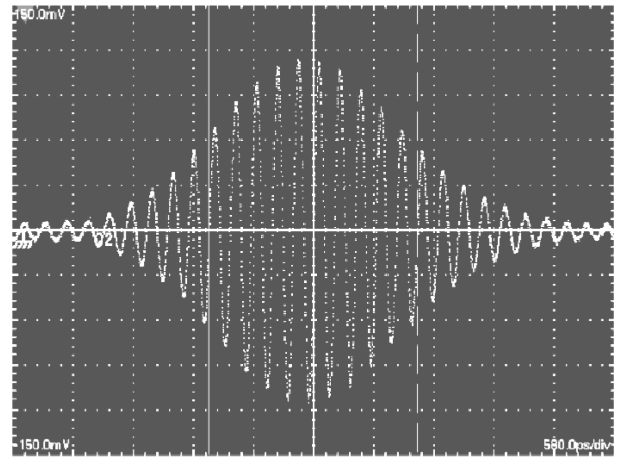
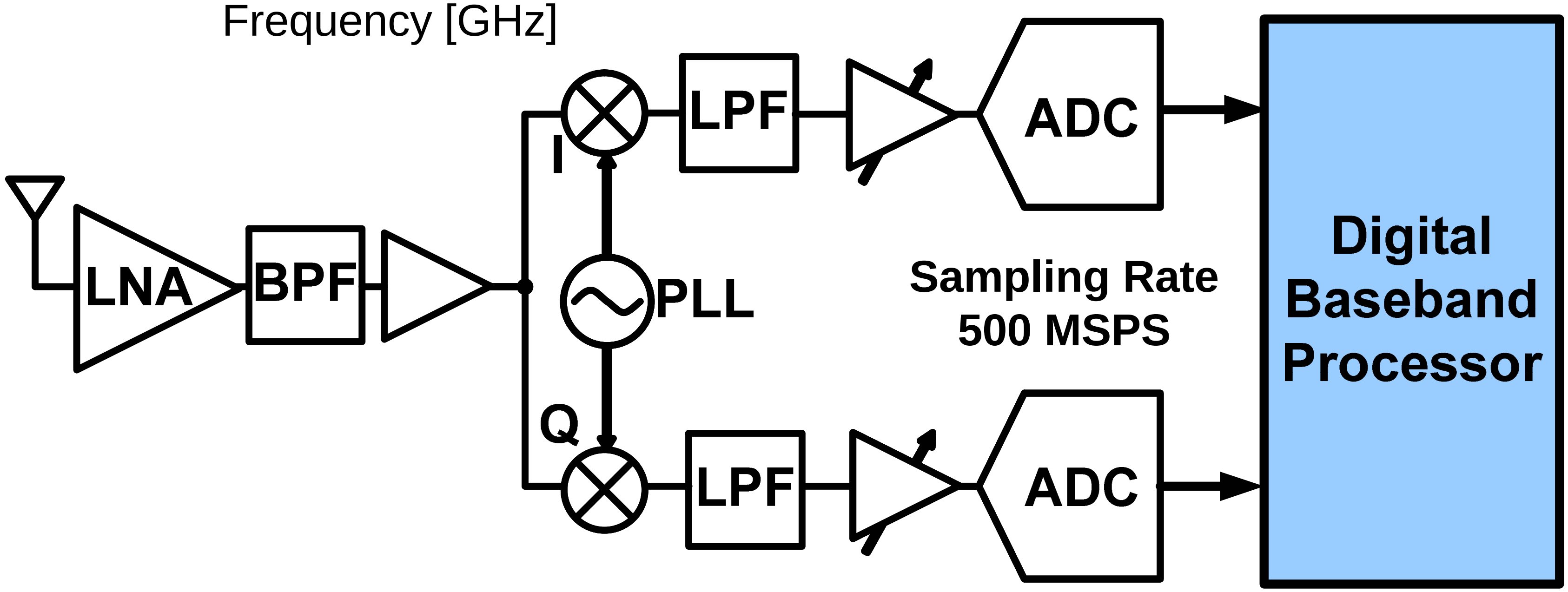
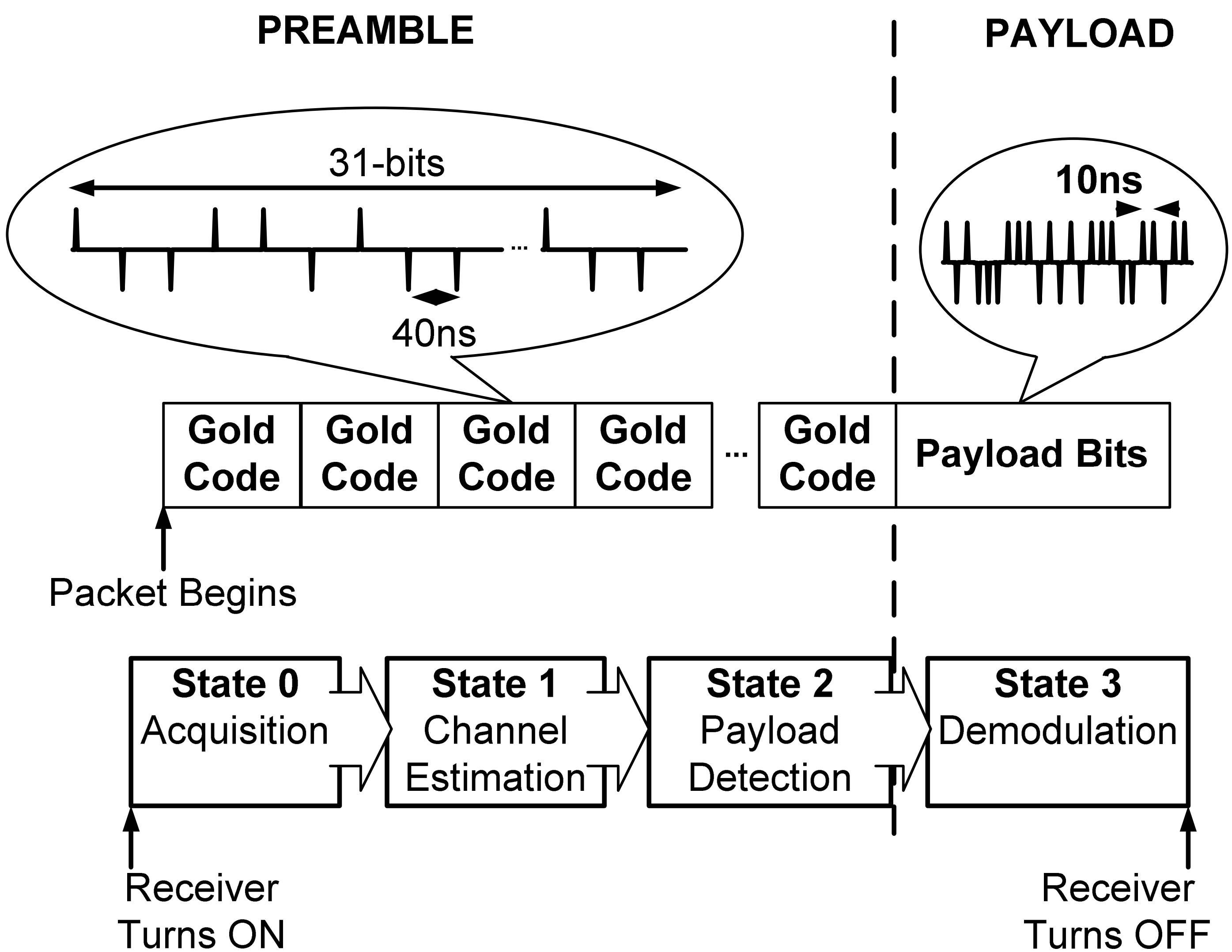


Figure courtesy of D.Wentzloff



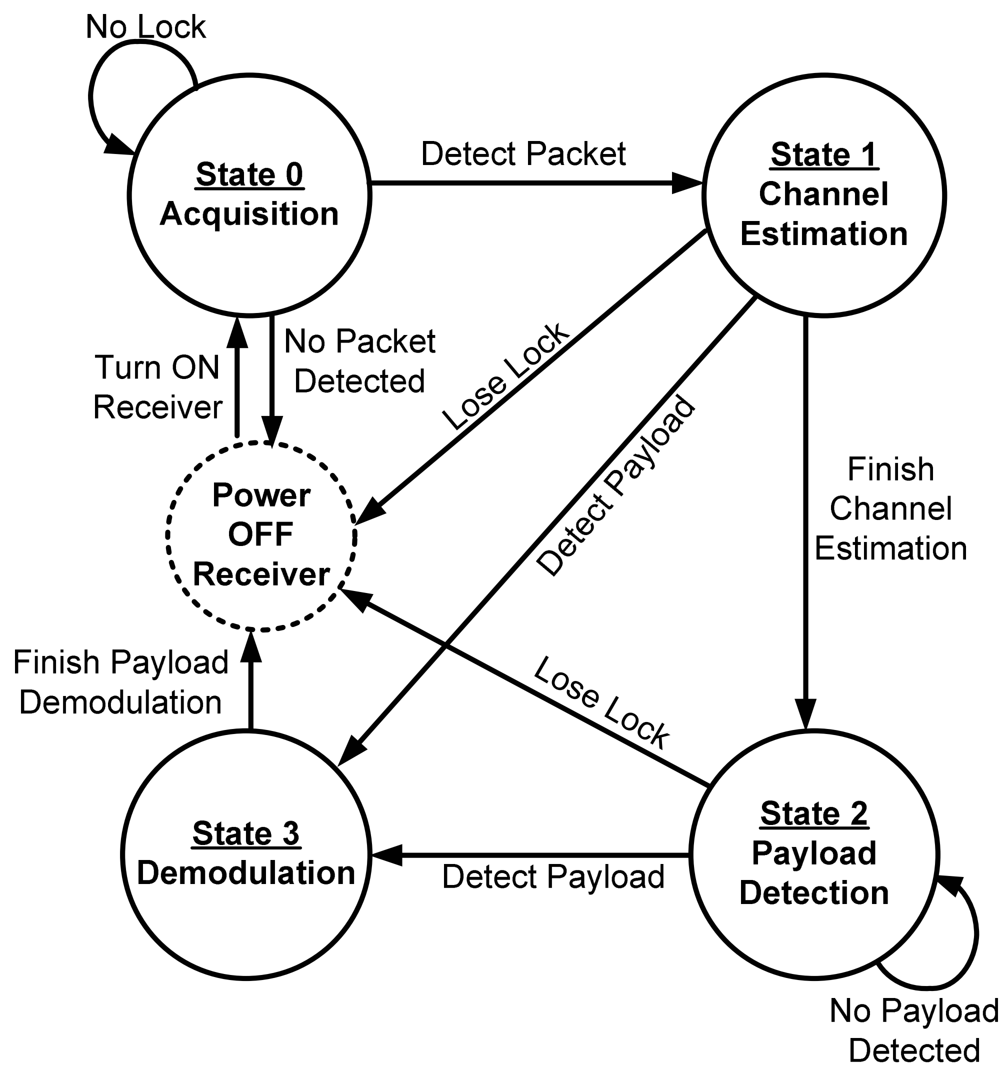
Packet Structure



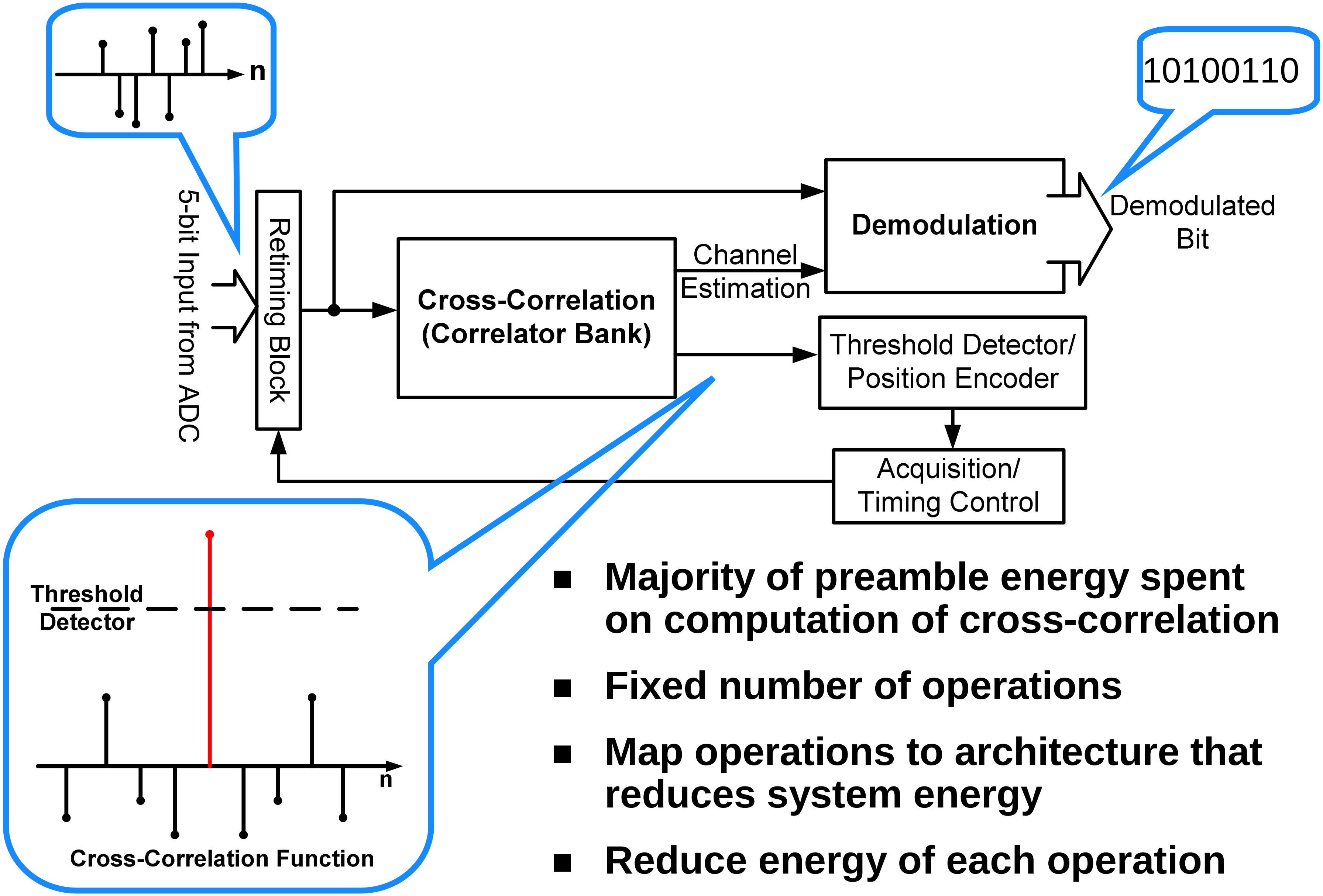
- **Goal : Reduce overhead energy (PREAMBLE)**

Baseband Algorithm

- **Acquisition Phase**
  - Detect packet
  - Estimate delay
  - Synchronize
- **Channel Estimation**
  - Measure multipath in wireless channel
- **Payload Detection**
  - Wait for inverted replication
- **Demodulation**
  - Adjust for multipath
  - Resolve bit



Baseband Architecture



- Majority of preamble energy spent on computation of cross-correlation
- Fixed number of operations
- Map operations to architecture that reduces system energy
- Reduce energy of each operation

Energy Efficiency Using Parallelism

Exploit <u>TWO</u> forms of parallelism in Correlator Bank

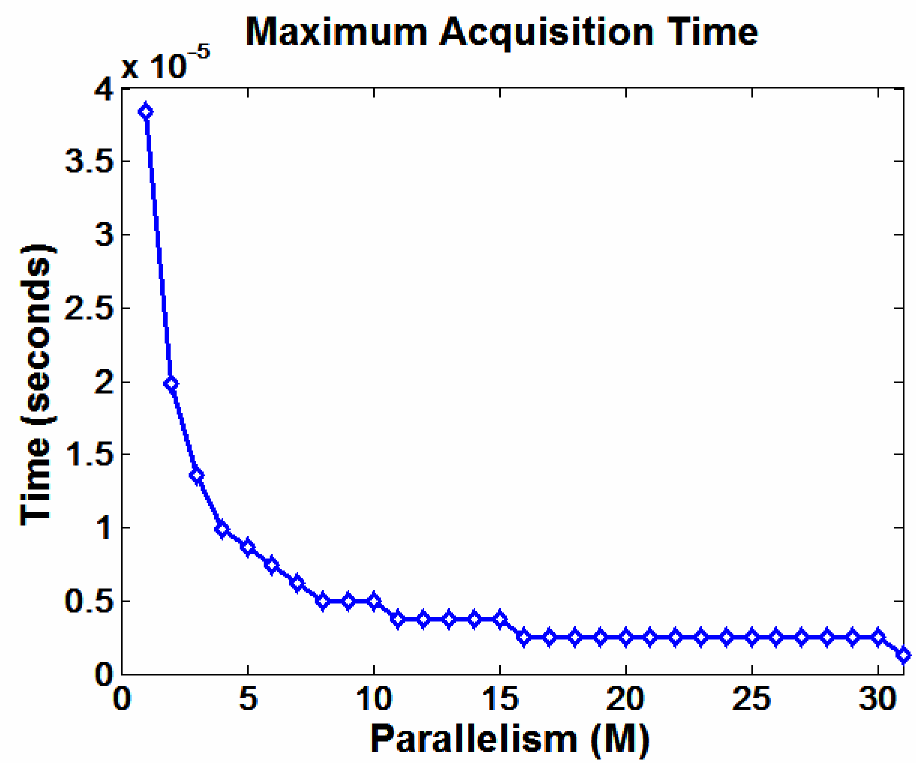
- **Mapping of Algorithm: Parallelized Computation (M)**
  - **Reduce acquisition time**
  - **Minimize System Energy (Energy per packet)**

- **Circuit Optimization: Maintain Throughput (L)**
  - **Reduce supply voltage**
  - **Minimize Baseband Energy (Energy per operation)**

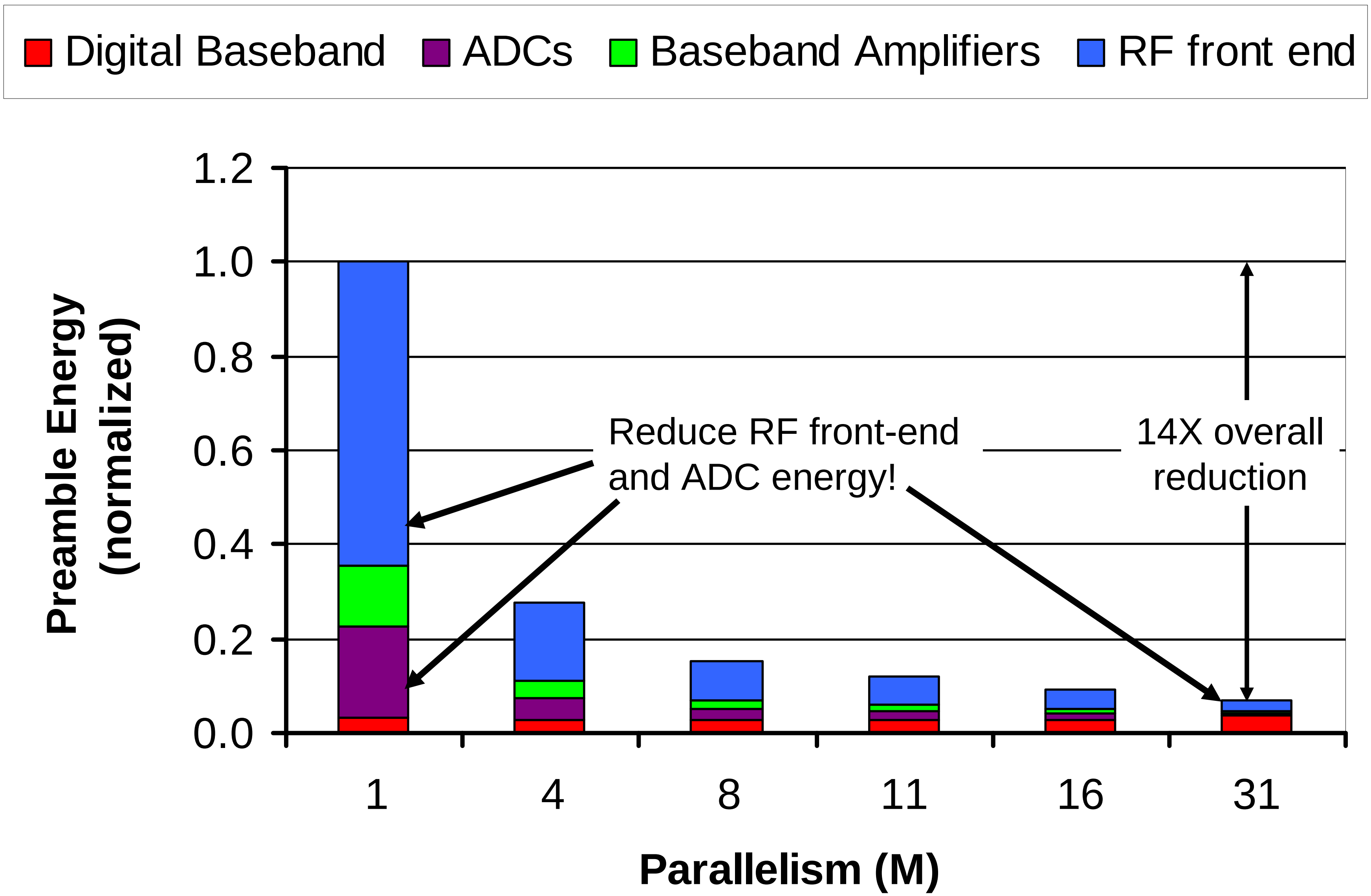
System Energy Savings (Mapping)

- **Trade-off area for time by mapping to parallel architecture**
- **Reducing acquisition time allows for fewer number of Gold Code repetitions in the preamble**
- **RF front-end and ADC can be turned off earlier**
- **<u>Energy savings across the entire system</u>**

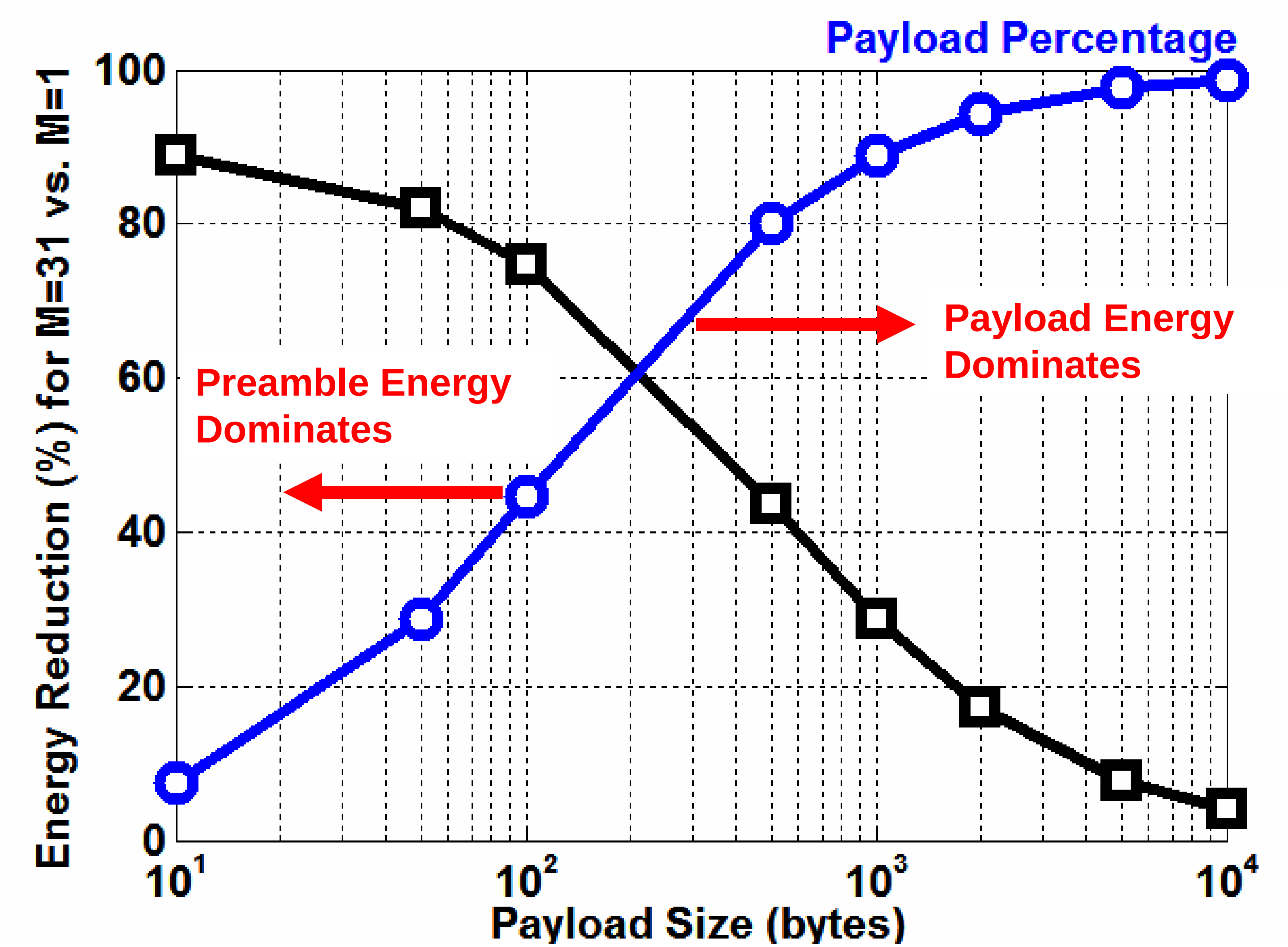
  → Reduce energy per packet



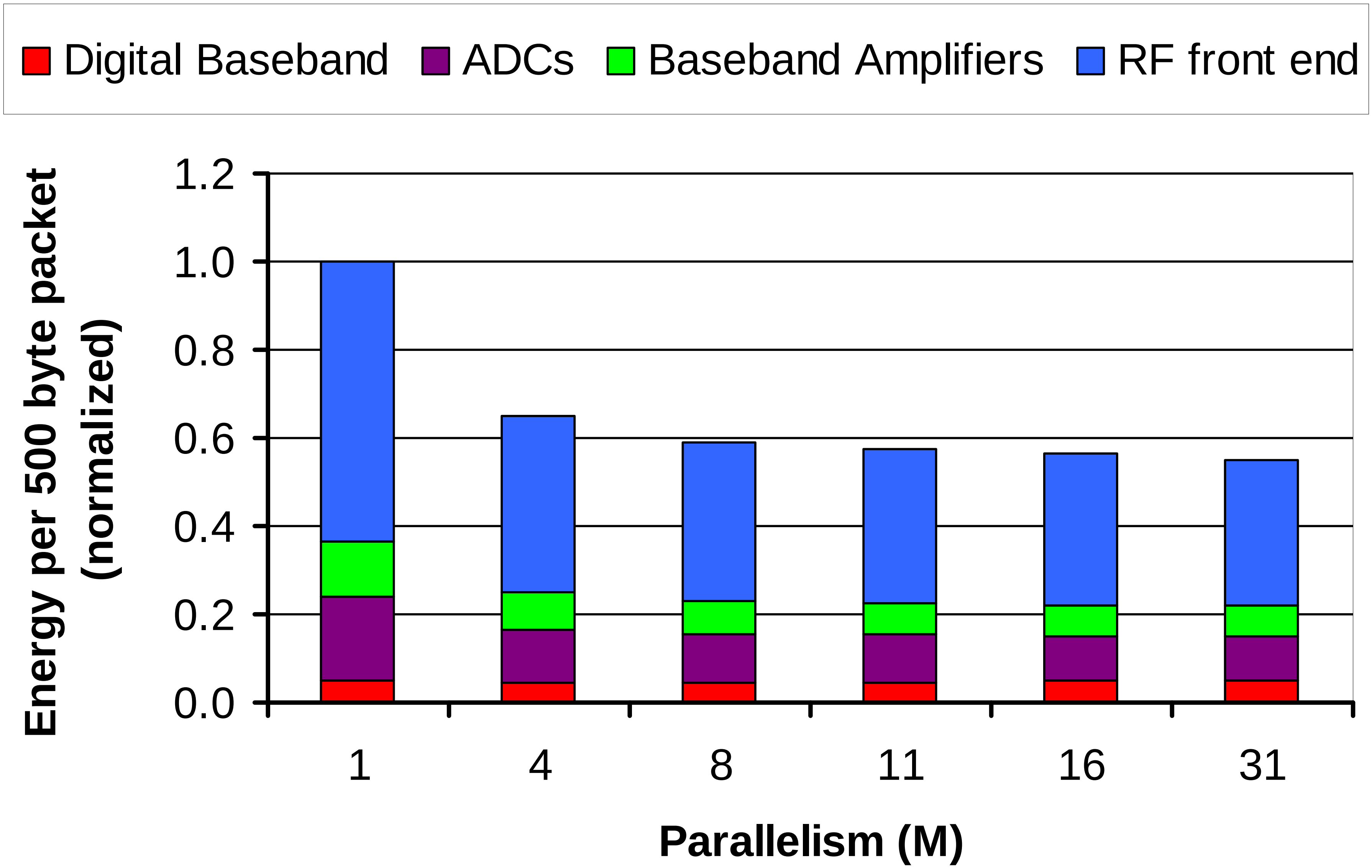
Preamble Energy Reduction



Energy Reduction vs. Payload Size

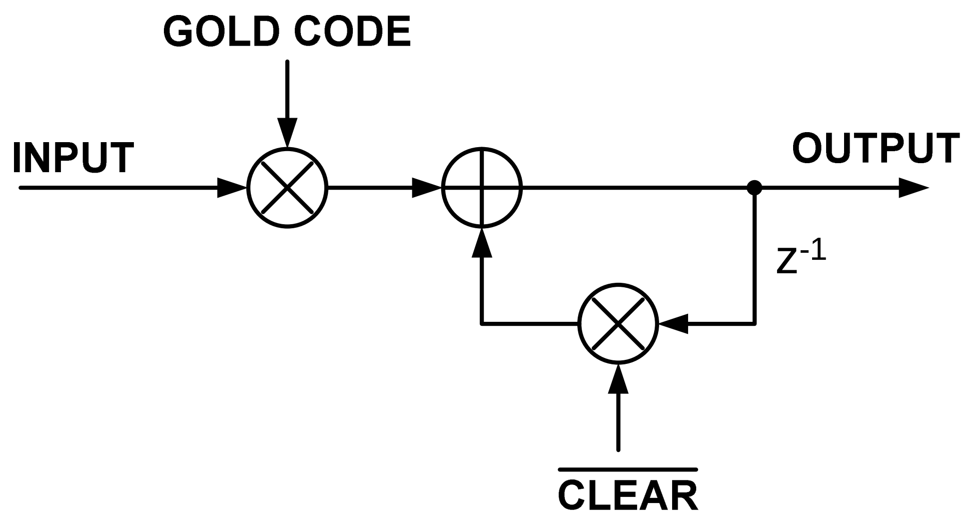


Total Packet Energy Reduction



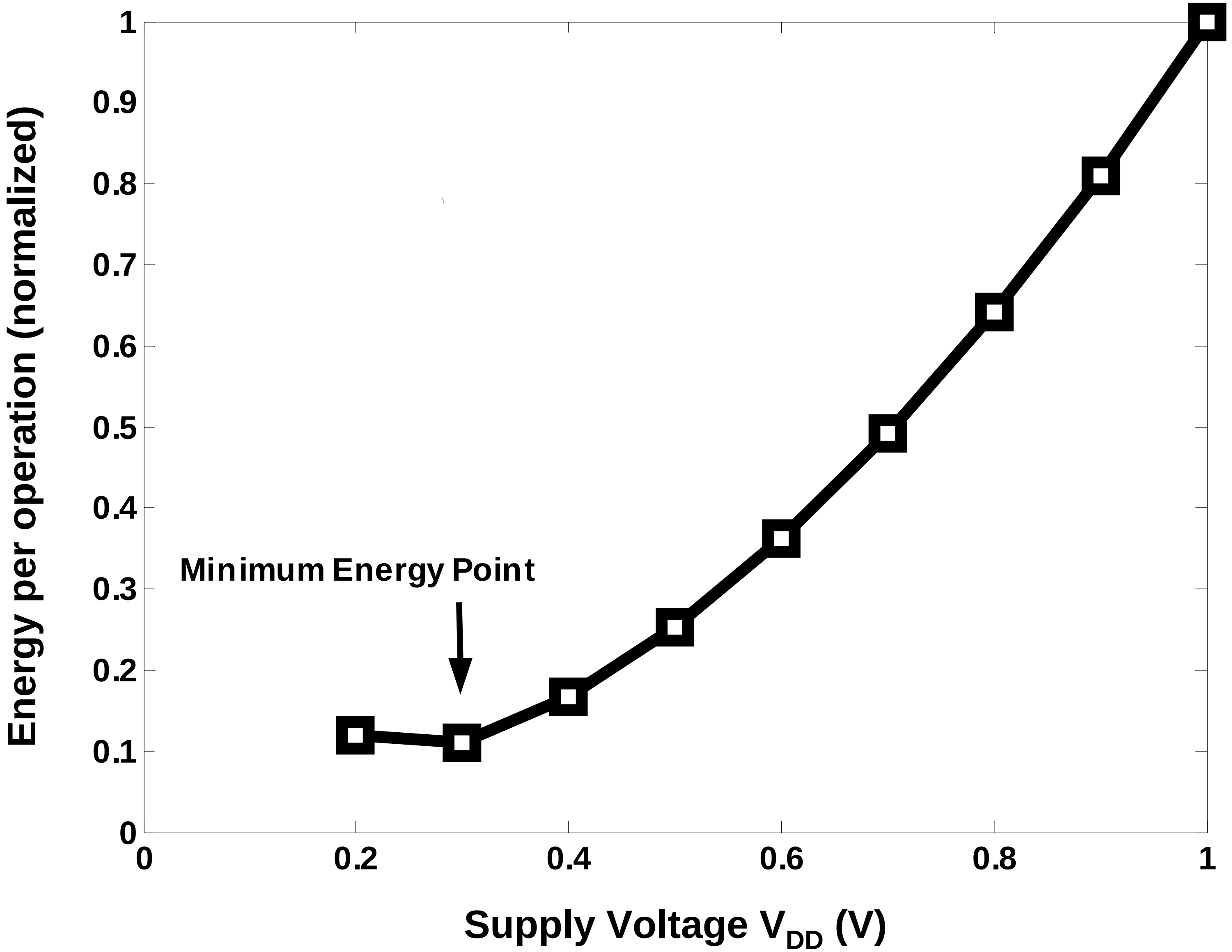
Baseband Energy Savings (Circuit Optimization)

Correlator Architecture



- Correlators compute the cross-correlation function
- Fixed number of operations required
- Voltage scale to reduce energy per operation
- Parallelize to maintain throughput of 500 MSPS
- Designed and simulated in a 90-nm process (STMicroelectronics)

Selection of Optimum Supply Voltage



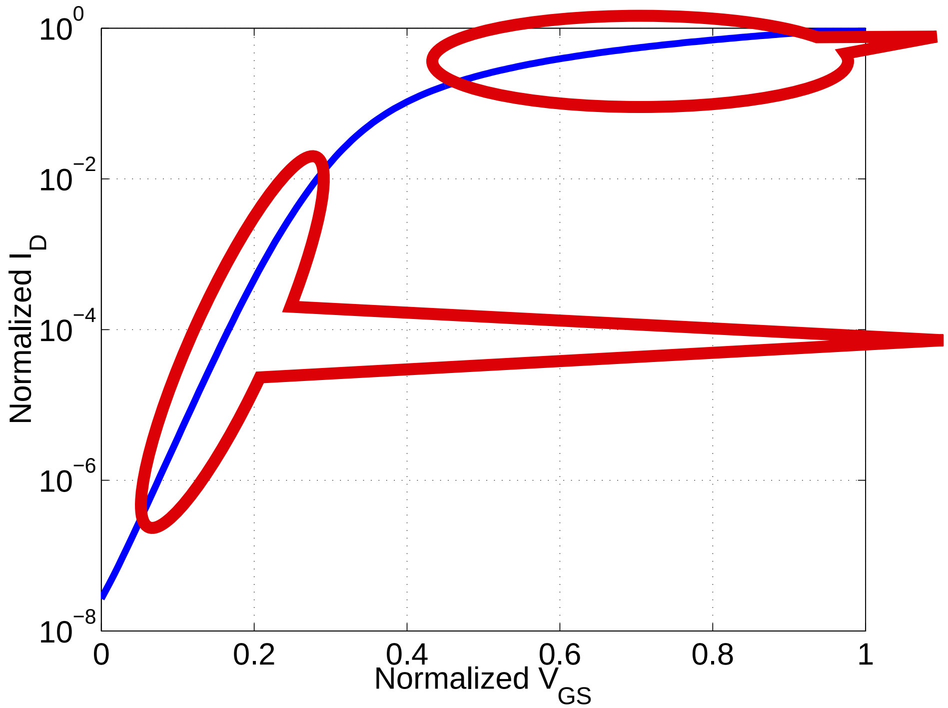
Minimum Energy Point

$$E_{dynamic} \propto C_{eff} V_{DD}^2$$

$$E_{leakage} \propto T_{period} V_{DD} I_{leak}$$

$$E_{total} = E_{dynamic} + E_{leakage}$$

Characteristic of typical NMOS device



Strong Inversion (V_{DD}> V_T)

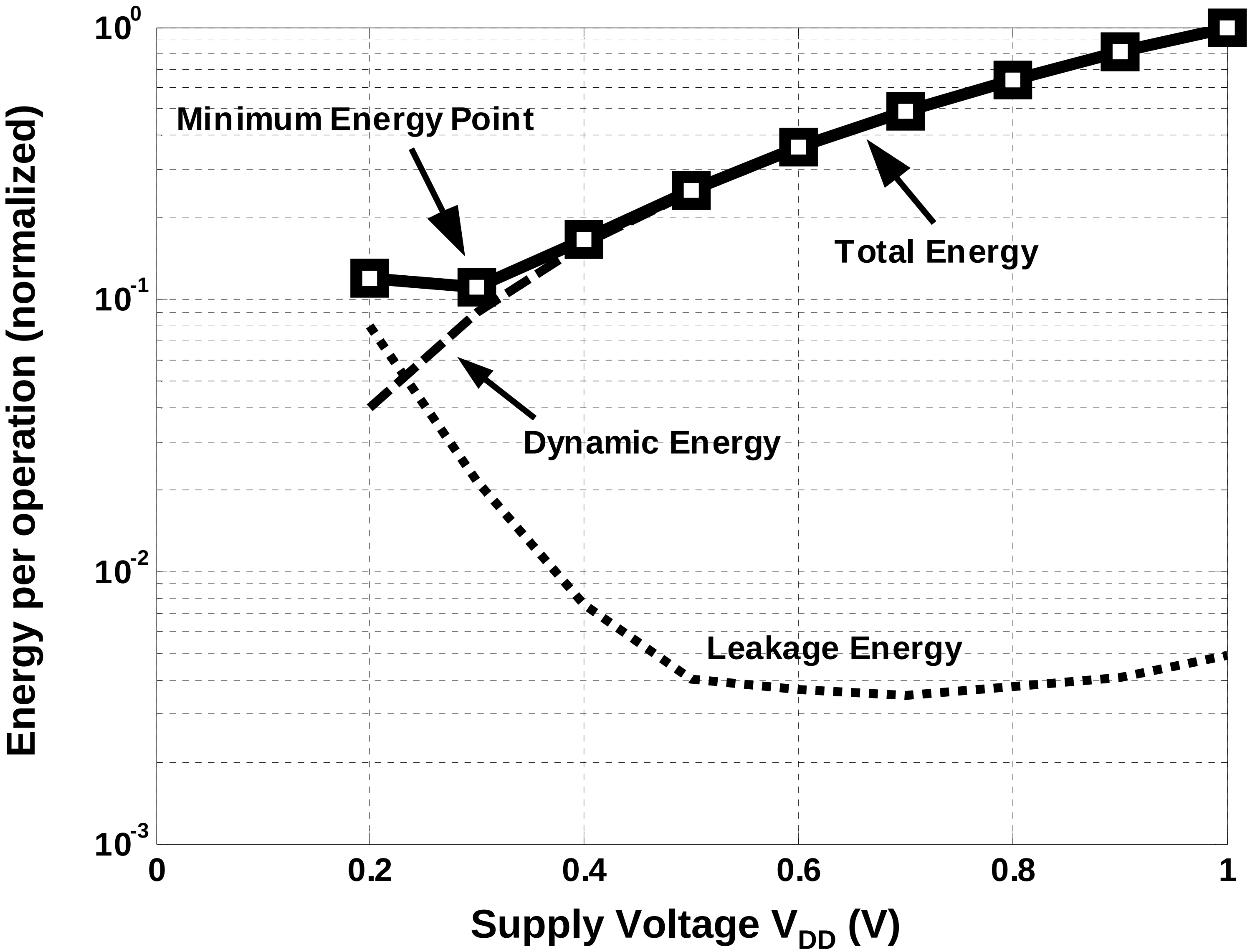
$$T_{period} \propto \frac{V_{DD}}{(V_{DD} - V_T)^2}$$

Sub-Threshold (V_{DD}< V_T)

$$T_{period} \propto \frac{V_{DD}}{e^{\frac{(V_{DD} - V_T)}{nkT/q}}}$$

for V_{GS}=V_{DD}

Correlator Energy per Operation



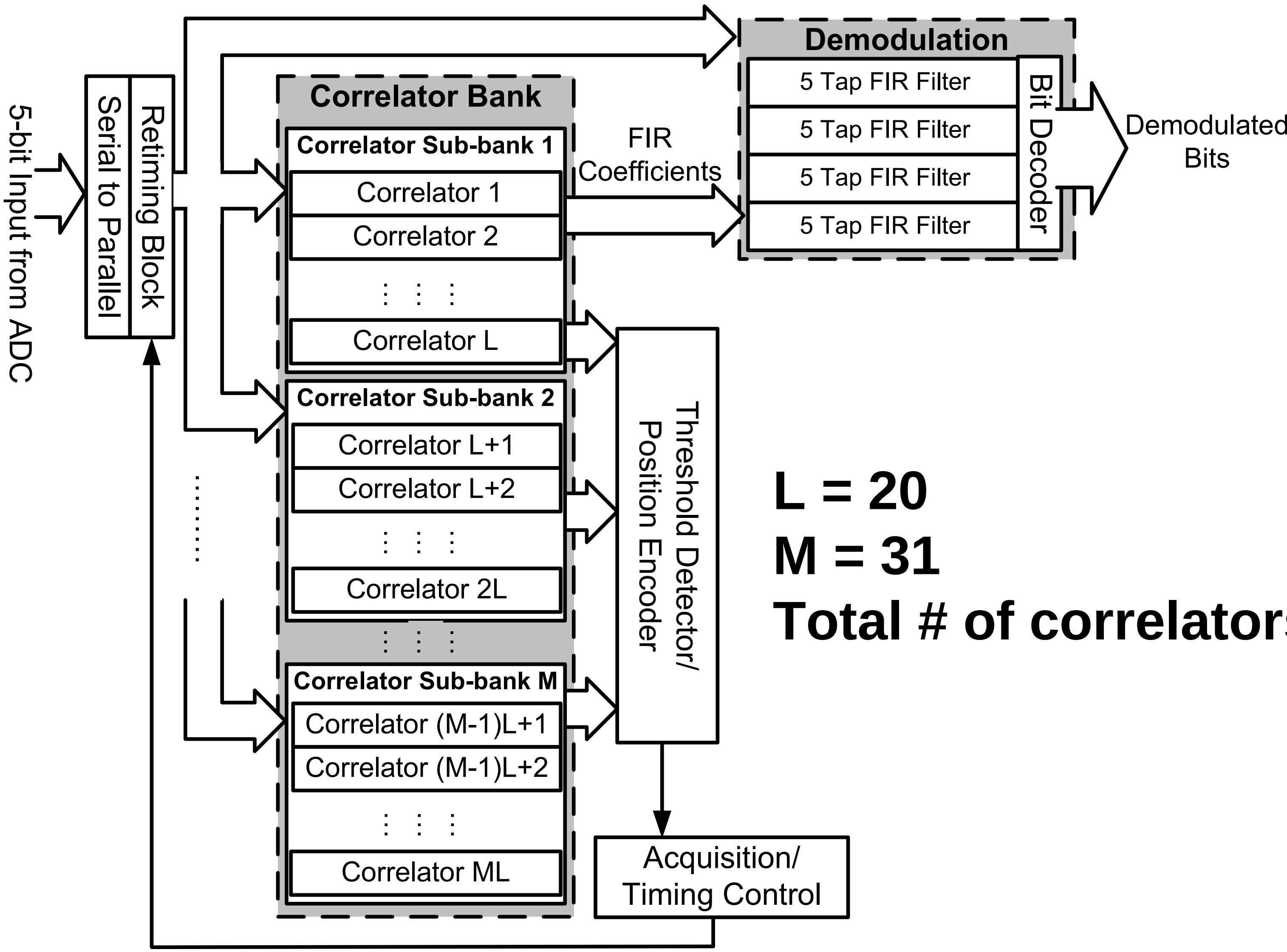
Baseband Energy Savings

- At the minimum energy point of 0.3 V

  → <u>reduce energy per operation by 9X</u>
- Set clock frequency to 25 MHz (preamble PRF)
- Parallelize by L=20 to maintain 500 MSPS throughput
- Need to raise voltage to 0.4 V to achieve 25 MHz
- At 0.4 V, <u>reduce energy per operation by 5.8X</u>

Minimum energy when baseband <u>operates in sub-threshold</u>

Parallelized Baseband Architecture



L = 20

M = 31

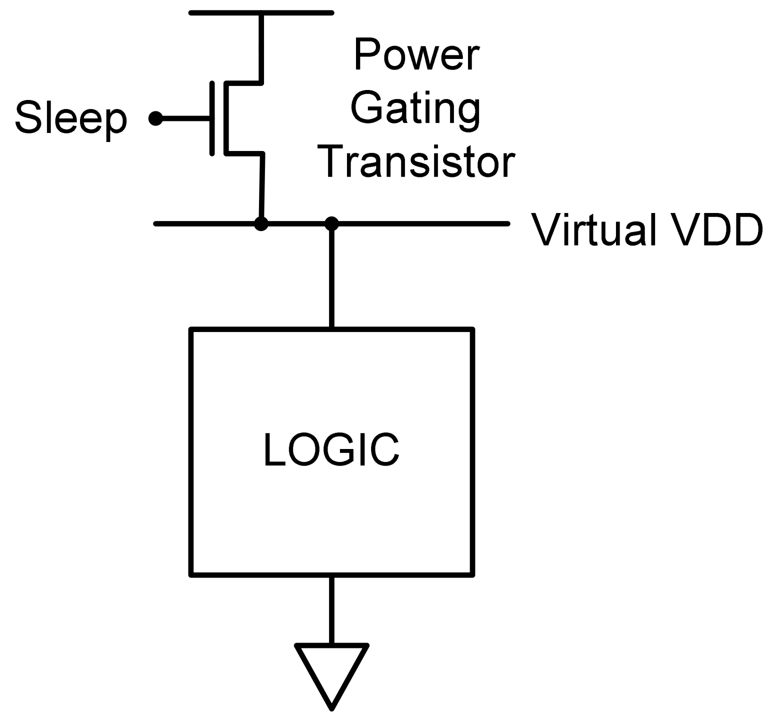
Total # of correlators = 620

Challenges with High Parallelism

- Major concerns for highly parallelized designs
  - Increased Leakage Current
  - Increased Interconnect Capacitance
- Use power gating to reduce leakage current
- Use clock gating and careful layout to reduce switching interconnect capacitance

Power Gating

- Larger number of transistors result in larger leakage currents
- Reduce leakage power by using a transistor to gate the leakage current when block is idle



Conclusions

- Reduce energy to receive a UWB packet by
  - Mapping algorithm to parallel architecture
  - Scaling to optimum supply voltage
- Reduced acquisition time
  - 14X reduction in preamble energy
  - 43% energy reduction for a 500 byte packet
- Voltage scaling to sub-threshold (1 V → 0.4 V)
  - 5.8X reduction in energy per operation of correlators
- This analysis can be applied to other high performance communication applications