A 47pJ/pulse 3.1-to-5GHz All-Digital UWB Transmitter in 90nm CMOS

David D. Wentzloff and Anantha P. Chandrakasan

Massachusetts Institute of Technology
Cambridge, MA

ISSCC 2007
Motivation

• Low-data rate, energy-constrained apps.

- Pulsed-UWB signaling inherently duty-cycled

TX and RX on only when a pulse is present

Fast (2ns) turn-on time

Data rate [b/s]

Energy/bit [J]

Trend:
Data rate ▼ Energy/bit ▲

[ISSCC]
System Specifications

- PPM signaling with non-coherent receiver
  - Variable frame time
  - Data encoded in pulse position
  - 30ns
- Three channel frequency plan
  - Each channel 550MHz wide
  - Center frequency: 6000ppm
- Self-mixing receiver
- Relaxed RF tolerance
- All-Digital Transmitter
Pulse Generation Principle

• Use a tapped variable delay line and edge combiner to synthesize a pulse

Equivalent to…

Positive Edge Combiner

Single modulated pulse

Center frequency depends on delay

Width depends on number of edges combined

Frequency selectivity without LO
Inverted pulse

Conventional PPM+BPSK

Randomly modulated PPM signals have spectral lines

PPM+BPSK scrambling eliminates tones

Conventional PPM+BPSK

Data $n$ pulse

Data $n+1$ pulse

Inverted pulse
Randomly modulated PPM signals have spectral lines.

PPM+Delay-Based BPSK scrambling eliminates tones in the main lobe.

Proposed PPM+DB-BPSK:

DB-BPSK: Minimal Overhead

0.5\(T_{RF}\) Delay
Transmitter Block Diagram

- PRF
- PRBS
- Edge Selection
- 30-Edge Combiner
- Feedback stage disabled when pulsing
- 32 stages, digital delay

Mask edges to combiner

Positive edge in ➤ one RF pulse out
Digital Delay Stage

Overall ±30% variation in delay → 8-bit delay control

Only selected edges are combined
Delay Line Calibration

Configure delay line as a ring oscillator

8-bit control

\[ f_{RING} = \frac{f_{RF}}{32} \]

Measure frequency by counting ring cycles

I0 I1 I2 I3 I4 I5
C0 C1

Measure frequency

Last current bit?

Choose current bit

Choose next current bit

Frequency in range?

Done

Select bank

Select current bit

Begin

Yes

No

Yes

No

Yes

4 banks

6 bits

Frequency in range?
Delay Range and Accuracy

Simulated RF Output

Frequency [GHz]

Digital Code

0 31 63 95 127 159 191 223 255

FF           TT           SS
Delay Range and Accuracy

Measured RF Output

Calibration Accuracy

Ring output is an accurate measure of pulse center frequency
30-Edge Combiner

Interleaved 15-edge combiners

15-Edge Combiner 1

15-Edge Combiner 2

XOR combiner outputs

To pad driver

Masked edges

[Kim, JSSC '02]

Edge to pulse

Q

\bar{Q}

Edge[1]

Edge[2]

A

B

x15

M2

M3

M4

[M1]
RF Pad Driver

From edge combiner

Standby

Weak pull-up

Linear-in-dB scaling

Stacked NMOS to reduce leakage

S11 in Idle State

27% efficiency
DB-BPSK Implementation

Per-stage delay is \( \frac{1}{2} \) RF period

Mask values offset by 1 bit

PRBS bit selects register

DB-BPSK Pulses

2.5ns

650mV

PPM + DB-BPSK Spectrum

PSD [dBm/MHz]

FCC Mask

PPM

PPM + DB-BPSK
## Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>90nm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active Area</td>
<td>0.2x0.4mm²</td>
</tr>
<tr>
<td>Modulation</td>
<td>PPM</td>
</tr>
<tr>
<td>Scrambling</td>
<td>DB-BPSK</td>
</tr>
<tr>
<td>Supply</td>
<td>1V</td>
</tr>
<tr>
<td>Leakage Power</td>
<td>96μW</td>
</tr>
<tr>
<td>Active E/pulse</td>
<td>37pJ/pulse</td>
</tr>
<tr>
<td>PRF Range</td>
<td>10kHz to 16.7MHz</td>
</tr>
<tr>
<td>Total E/bit</td>
<td>9.6nJ/bit to 43pJ/bit</td>
</tr>
</tbody>
</table>

- Energy consumed in sub-$V_t$ leakage and $CV^2$
- Digital architecture practical for non-coherent RX

Acknowledgements – MARCO/DARPA Focus Center for Circuit & System Solutions (C2S2), National Science Foundation (NSF), and STMicroelectronics for chip fabrication