A 0.4-V UWB Baseband Processor

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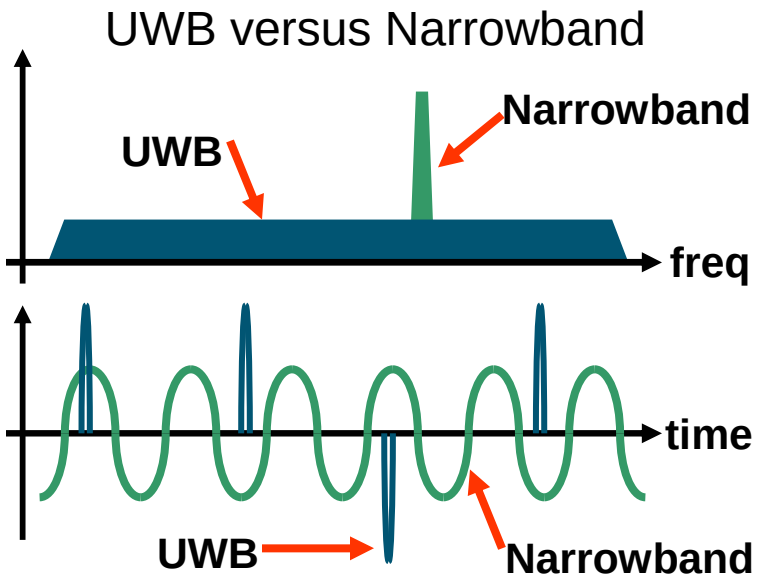
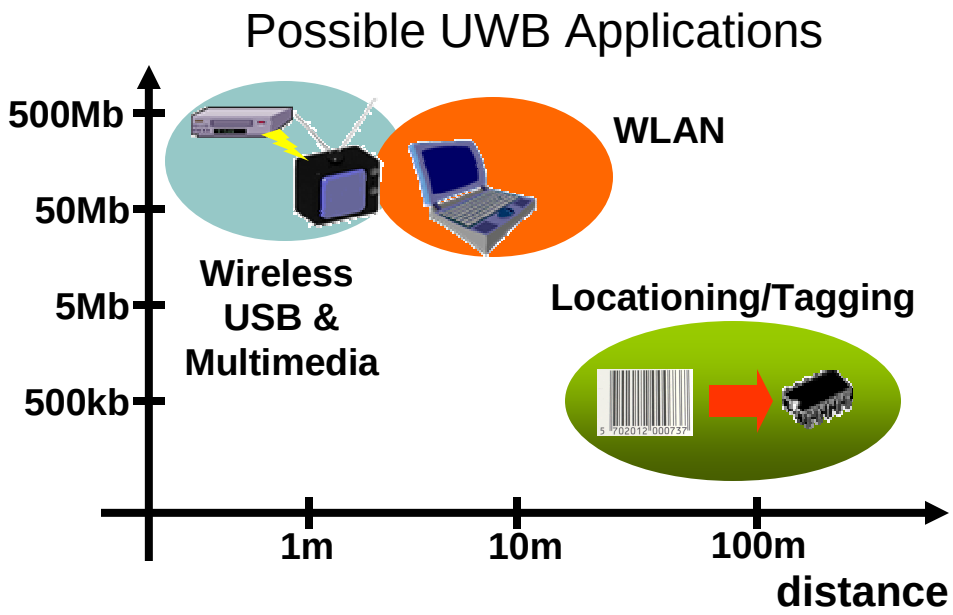
Outline

- UWB Specifications and System Architecture
- Baseband Algorithm and Architecture
- Parallelism for Energy Efficiency
  - aggressive voltage scaling
  - reduced receiver on-time
- Chip Measurements
- Conclusions

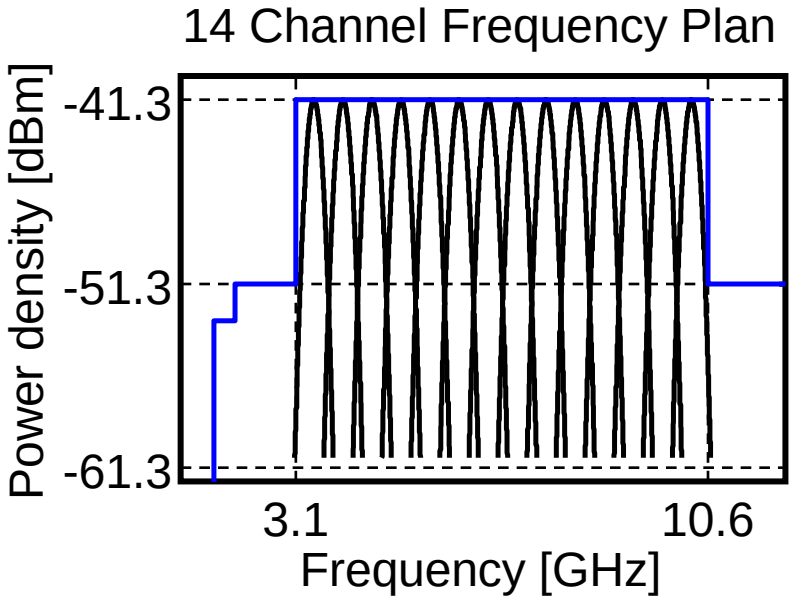
Ultra-wideband (UWB) Radio





- Advantages of UWB communications include
  - High Data Rate
  - Excellent Multi-path Resolution
  - Low Interference
- Integrate UWB radios on battery operated devices
- Need an energy efficient UWB System

UWB System Architecture



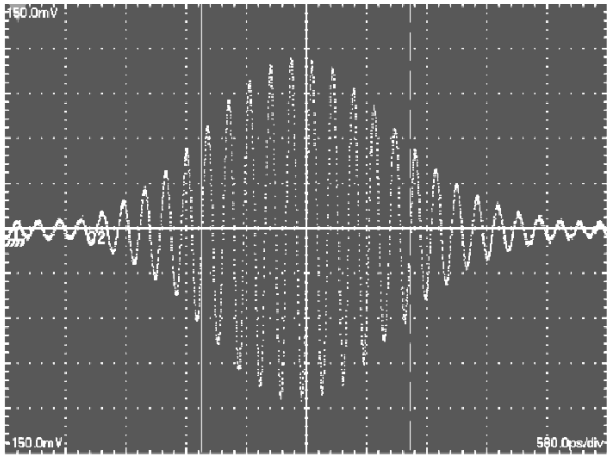
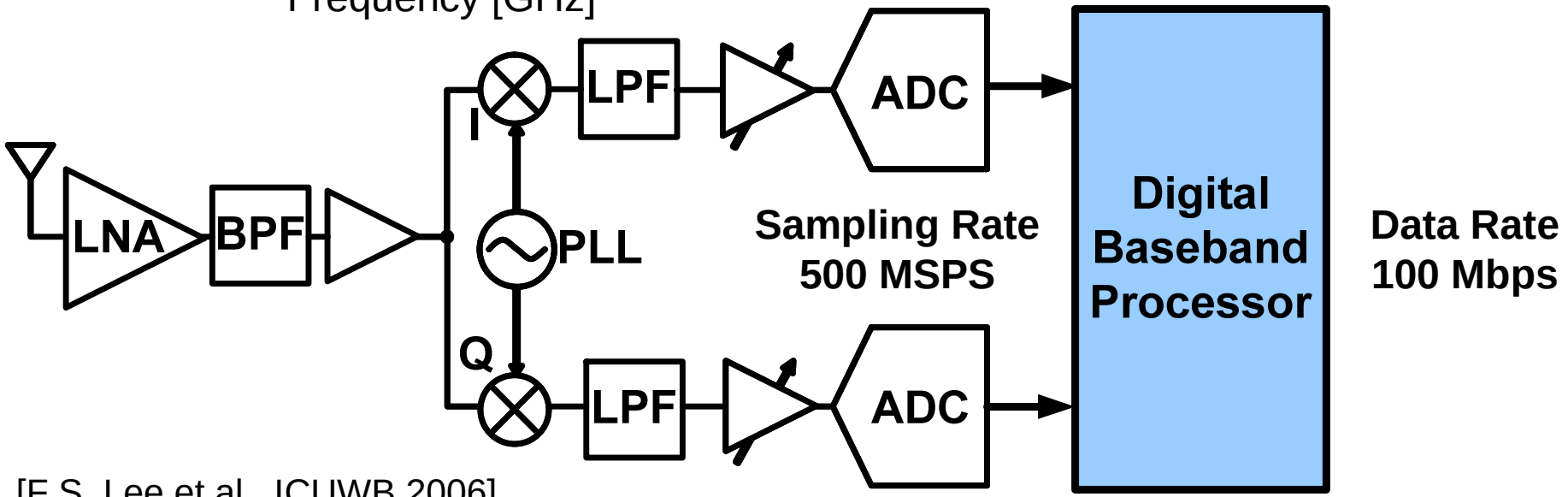
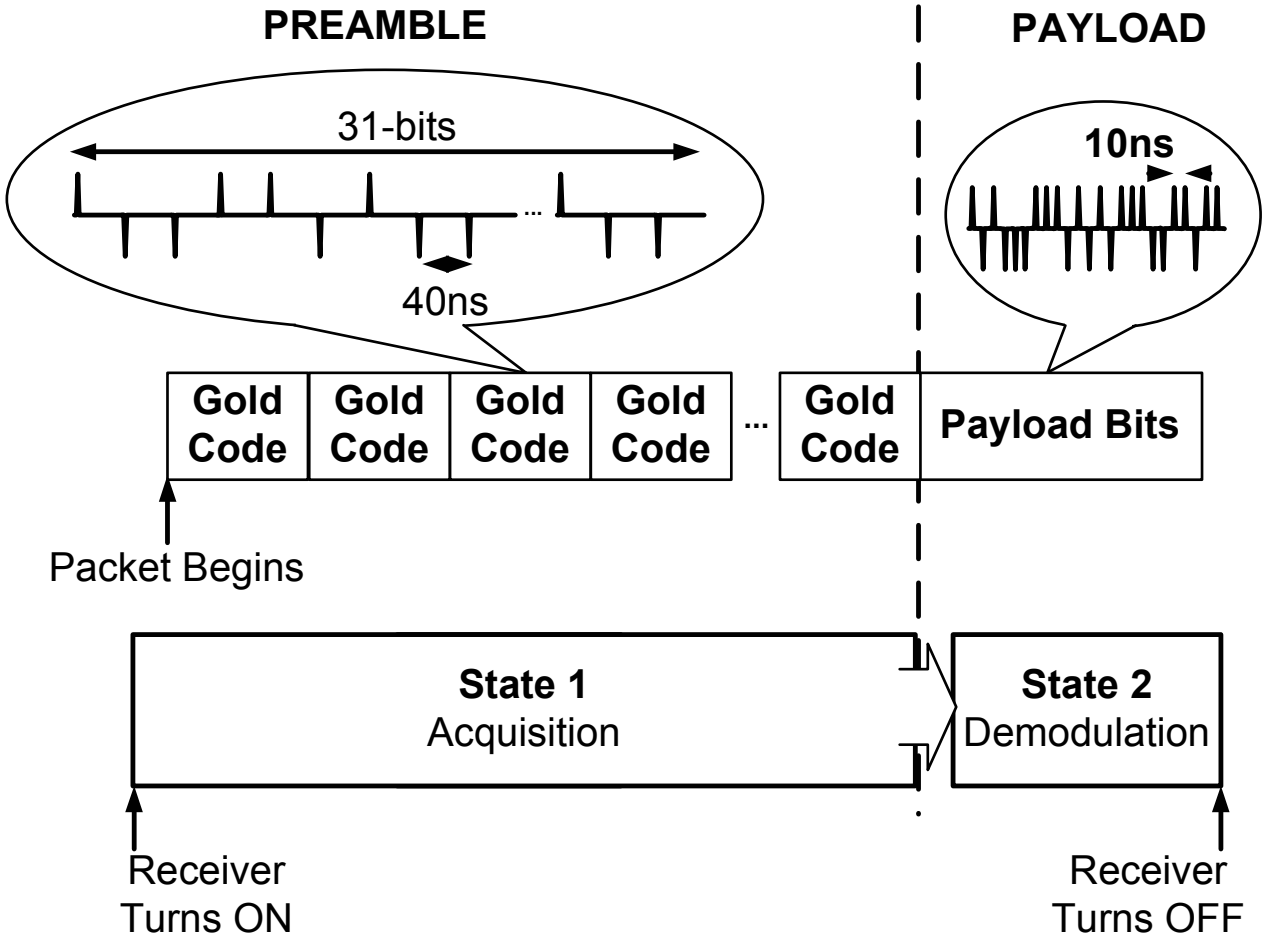


Figure courtesy of D.Wentzloff



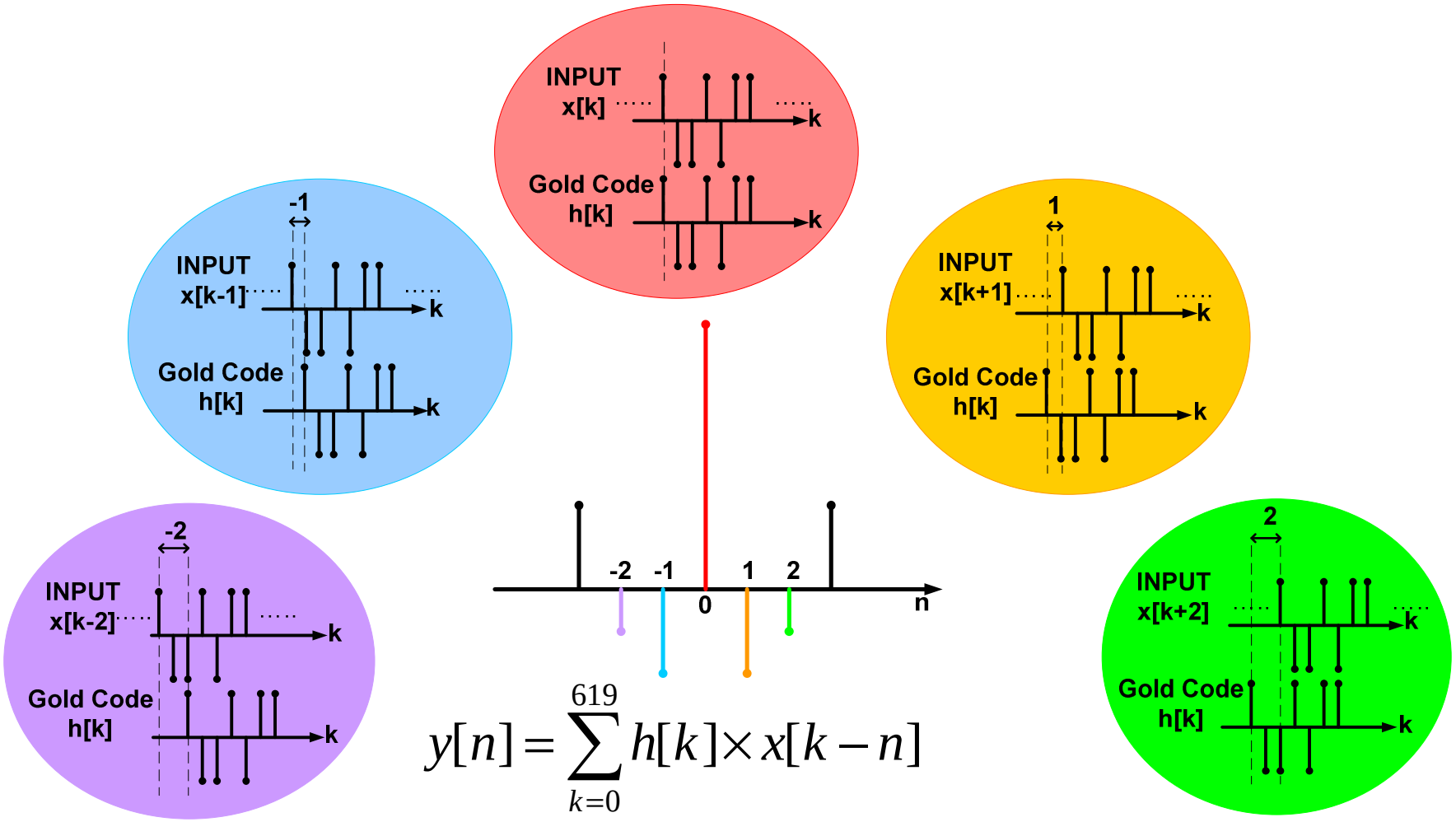
[F.S. Lee et al., ICUWB 2006]

Packet Structure (PHY layer)



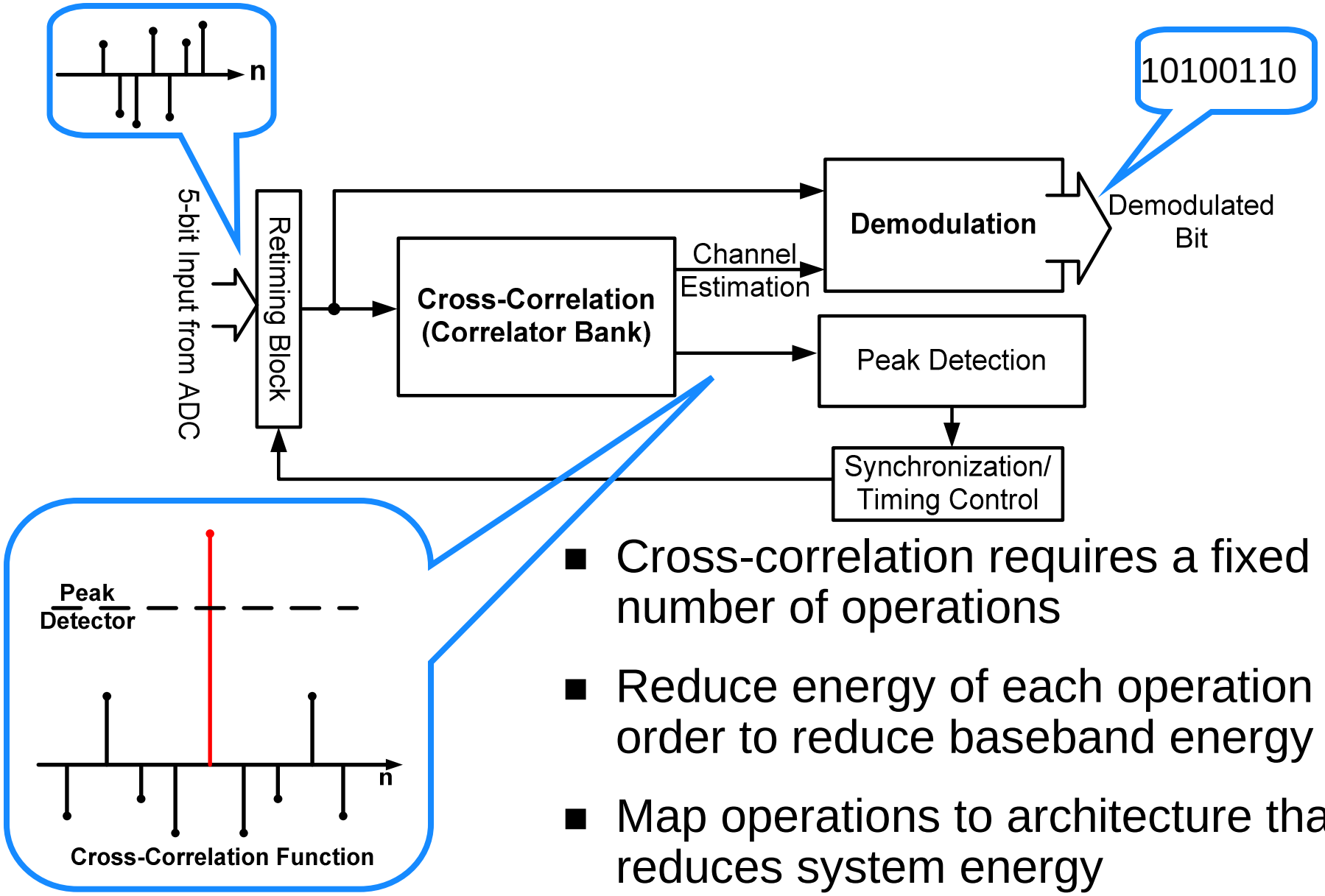
- Goal : Reduce overhead energy (acquisition)
- Majority of acquisition energy spent on computation of cross-correlation

Cross-Correlation Computation



- Points can be computed independently

Baseband Architecture



- Cross-correlation requires a fixed number of operations
- Reduce energy of each operation in order to reduce baseband energy
- Map operations to architecture that reduces system energy

Energy Efficiency Using Parallelism

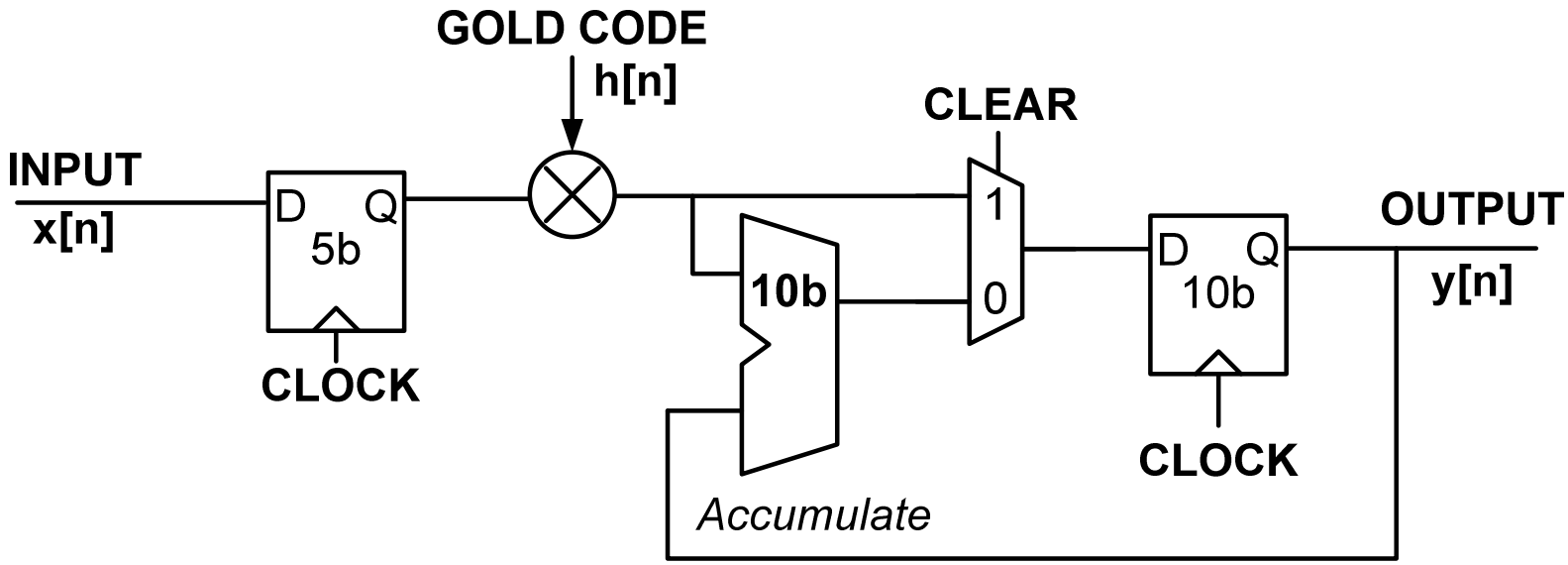
Exploit **TWO** forms of parallelism in Correlator Bank

- Ultra-Low Voltage Operation - Maintain Throughput (L)
  - Reduce supply voltage
  - Minimize energy of baseband processor
- Reducing Acquisition Time - Parallelized Computation (M)
  - Reduce receiver on-time
  - Minimize energy of entire receiver (system)

Baseband Energy Savings

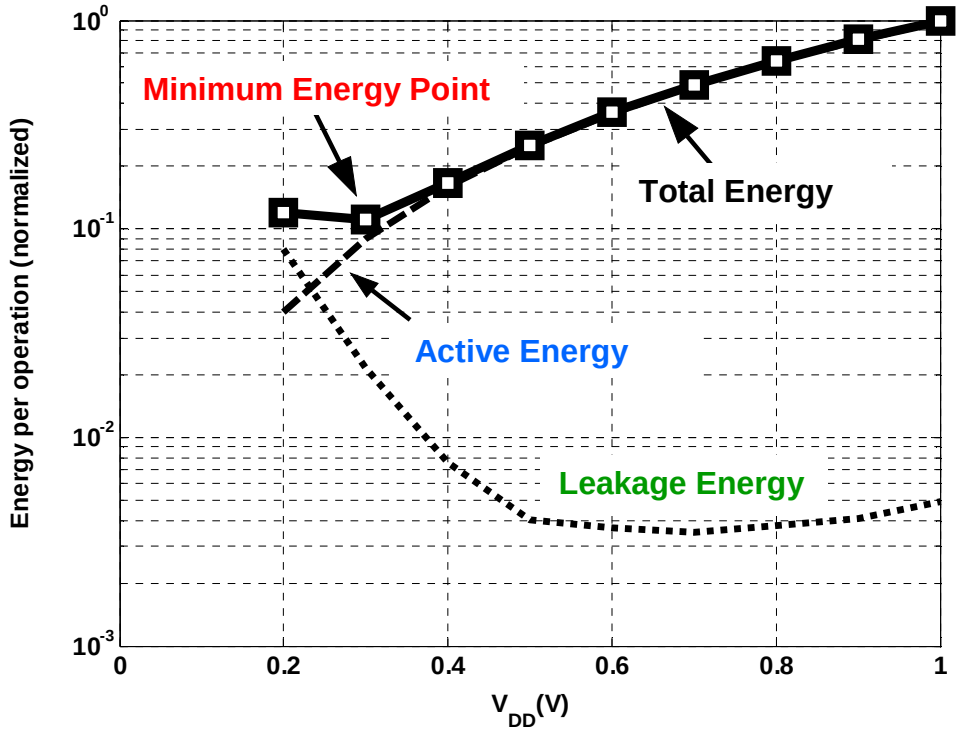
Correlator Architecture

$$y[n] = \sum h[k] \times x[k-n]$$



- Correlators compute the cross-correlation function
- Voltage scaling to reduce energy per operation
- Parallelize to maintain throughput of 500 MSPS
- Designed and simulated in a 90-nm process

Baseband Energy Savings



- At the **minimum energy point of 0.3 V** → 9X energy reduction
- Set clock frequency to 25 MHz (preamble PRF)
- Parallelize by L=20 to maintain 500 MSPS throughput
- Need to raise voltage to 0.4 V to achieve 25 MHz
- **At 0.4 V, reduce energy per operation by 5.8X**

$$E_{total} = E_{active} + E_{leakage}$$

$$E_{active} \propto C_{eff} V_{DD}^2$$

$$E_{leakage} \propto T_{period} V_{DD} I_{leak}$$

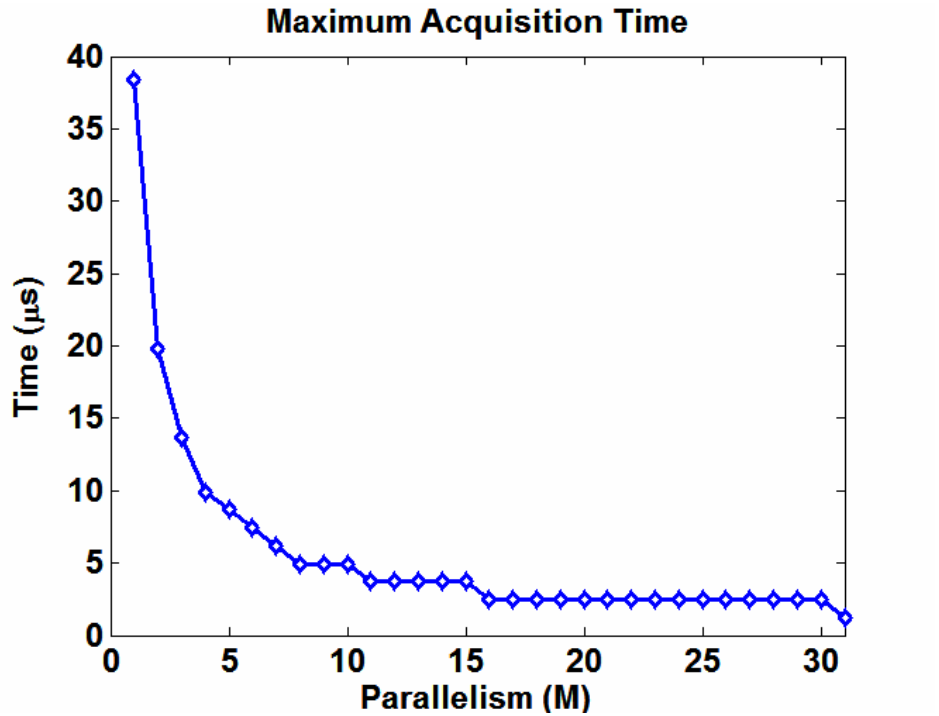
Summary of Methodology

- Select the optimal degree of parallelism that
  - **minimizes energy consumption**
  - **meets performance constraints**

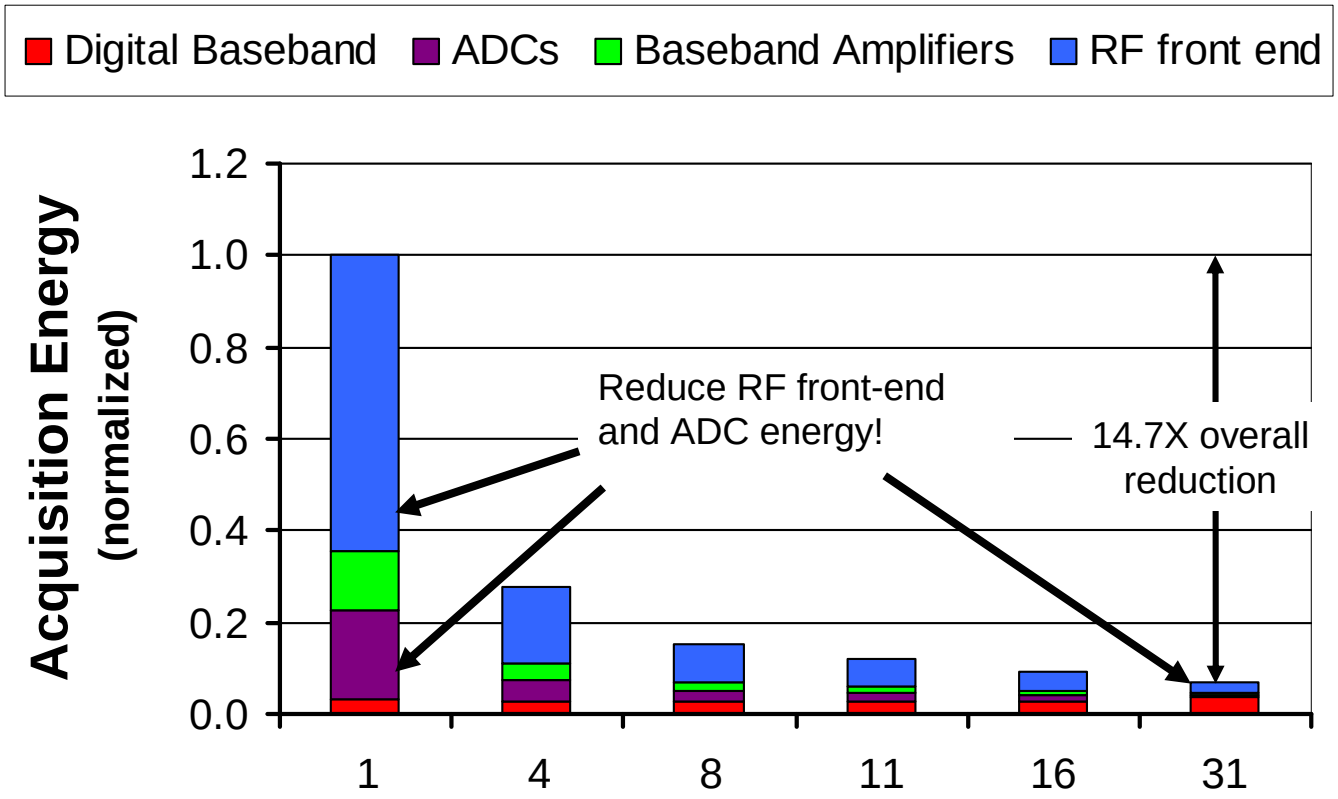
1. Determine VDD_{MEP} (at minimum energy point)
2. Determine delay and throughput at VDD_{MEP}
3. Divide required throughput by the throughput at VDD_{MEP} to obtain the necessary degree of parallelism (L)

System Energy Savings

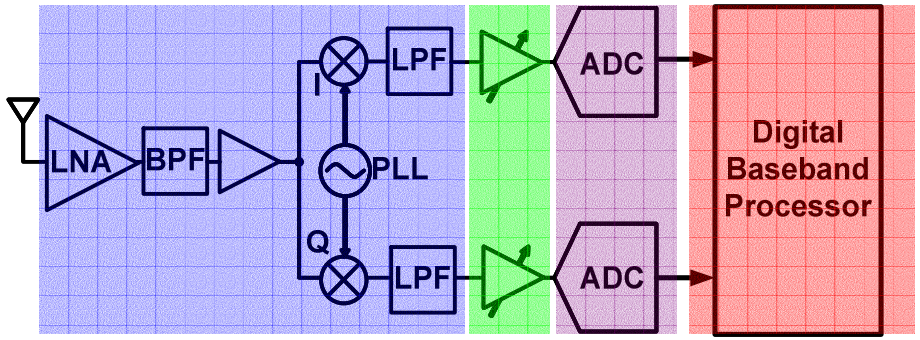
- Trade-off area for time by mapping to parallel architecture
- Reducing acquisition time allows for fewer number of Gold Code repetitions in the preamble
- RF front-end and ADC can be turned off earlier
- **Energy savings across the entire system**



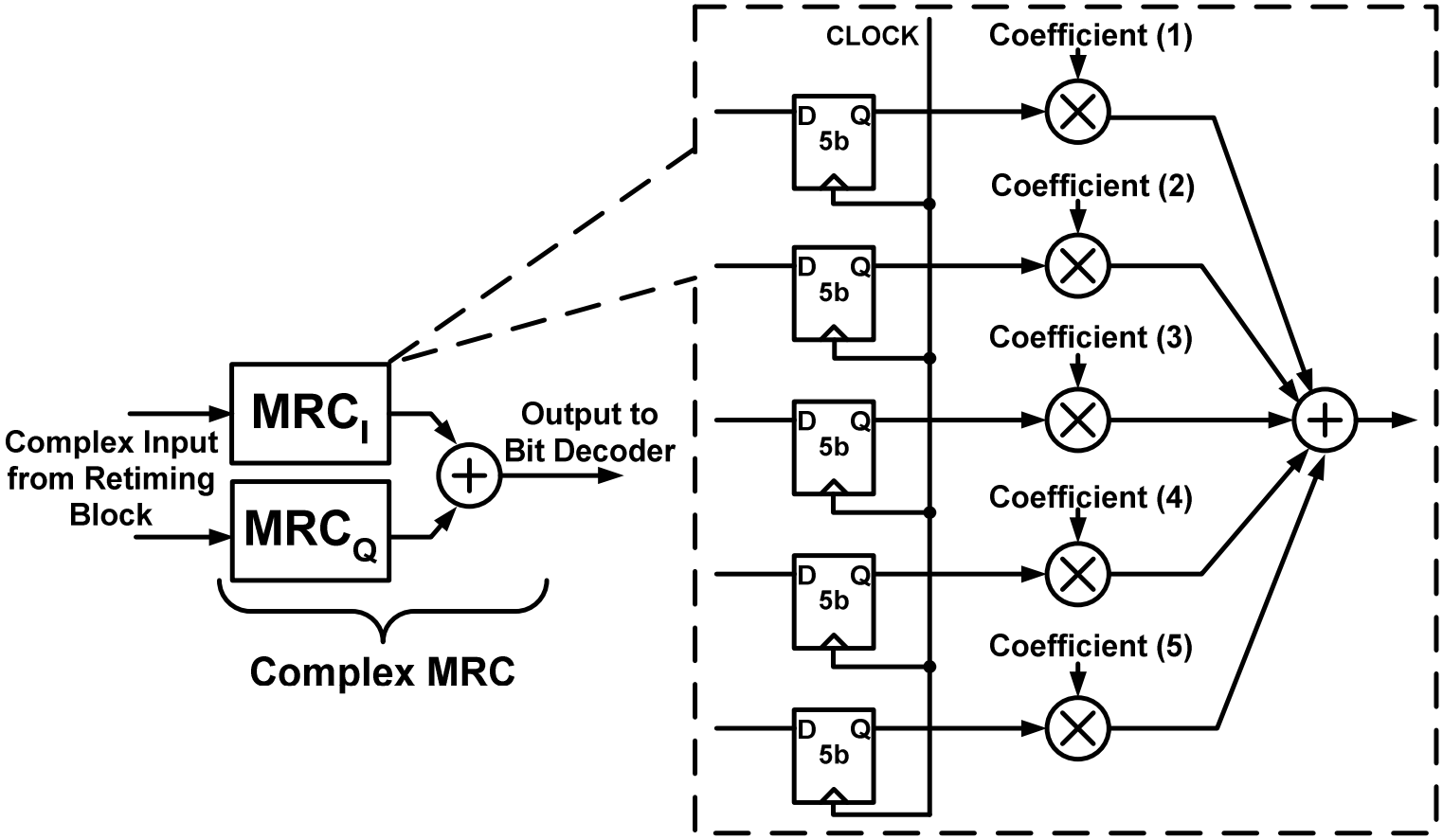
Acquisition Energy Reduction



[V. Sze, R. Blázquez, M. Bhardwaj, A. Chandrakasan, ICASSP 2006.]

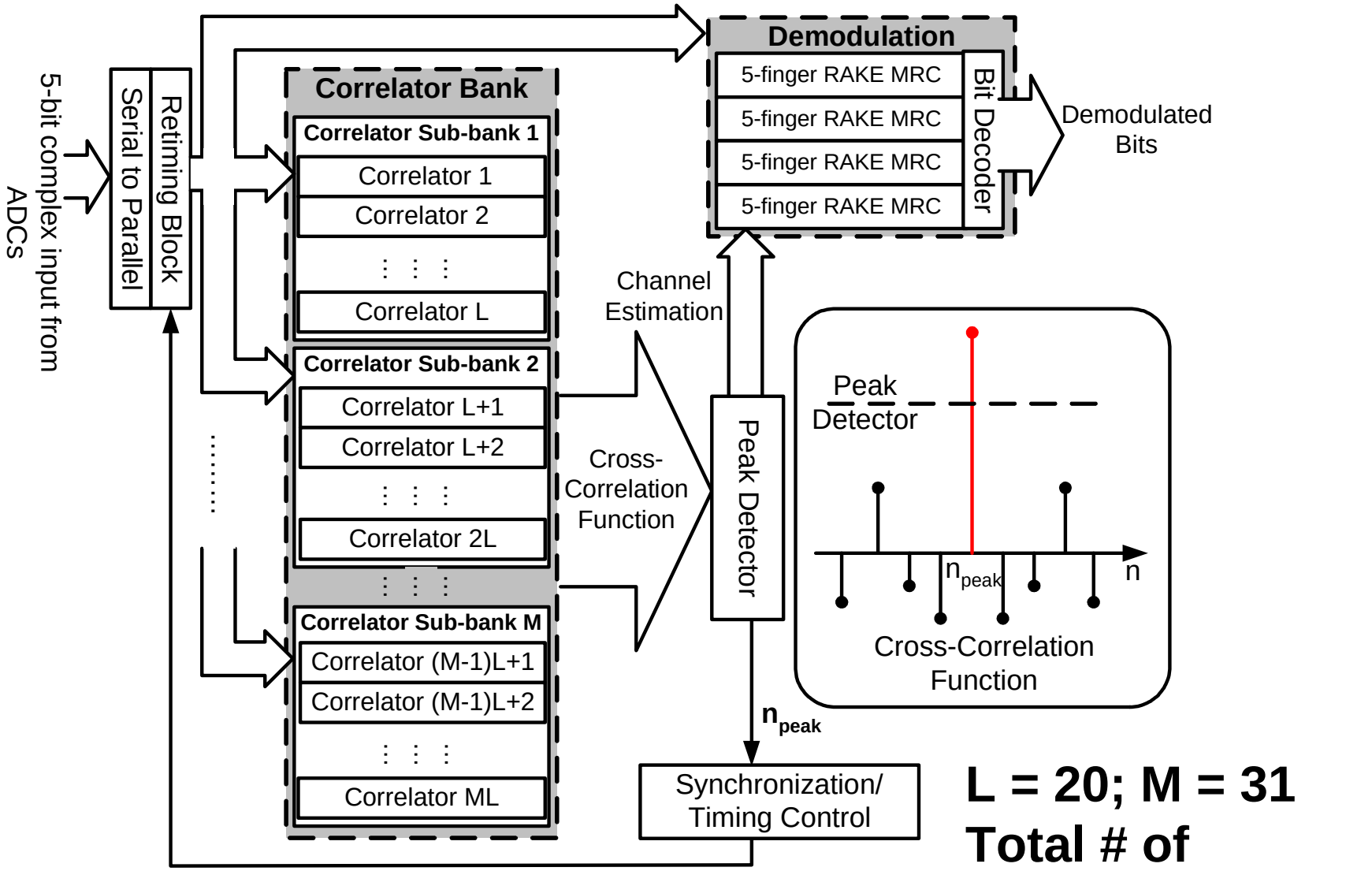


Maximum Ratio Combiner (MRC)



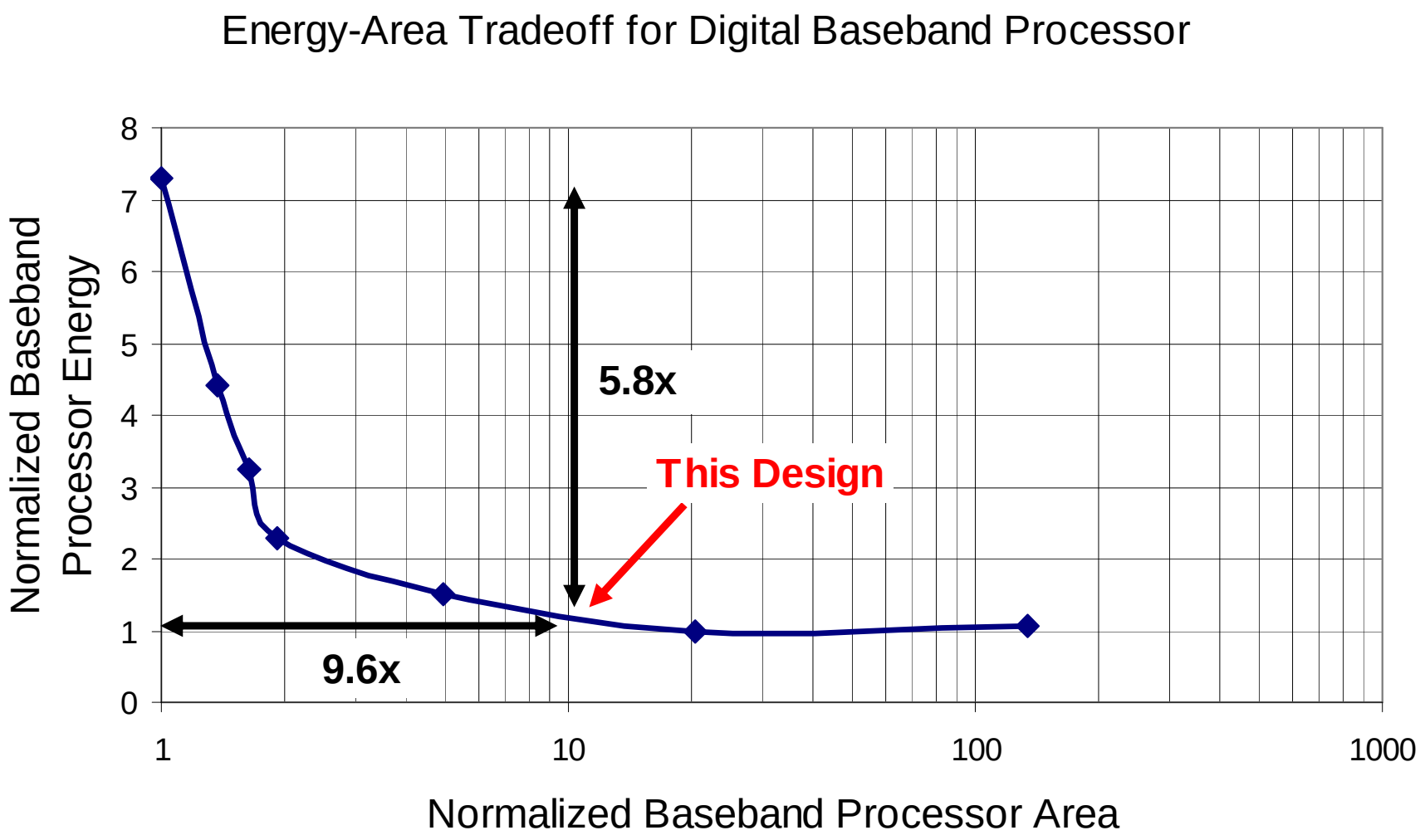
- Demodulation uses a 5-fingered RAKE receiver
- A hard decision is made at the output MRC to resolve a bit

Parallelized Baseband Architecture

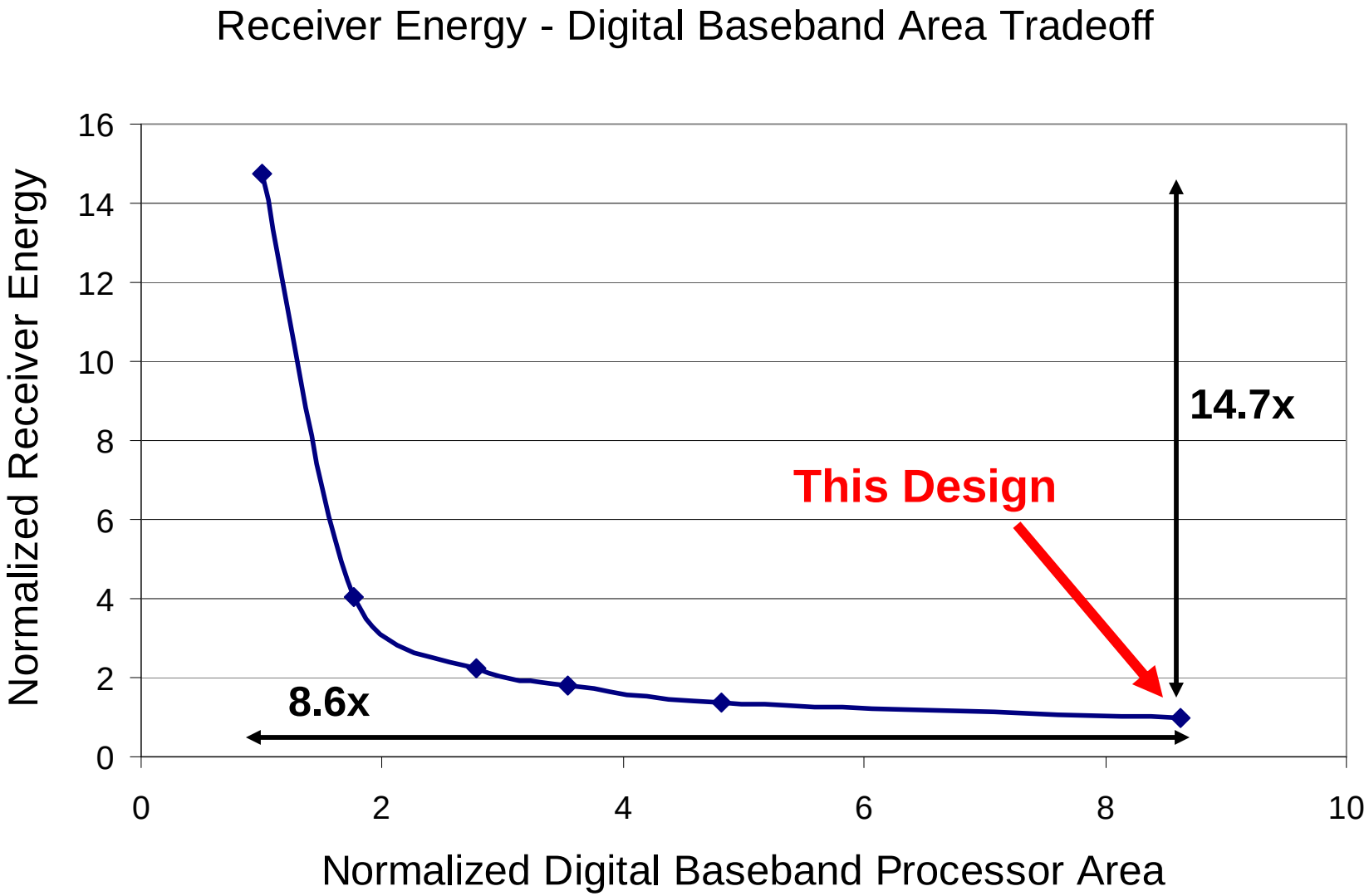


L = 20; M = 31
Total # of correlators = 620

Energy-Area Tradeoff

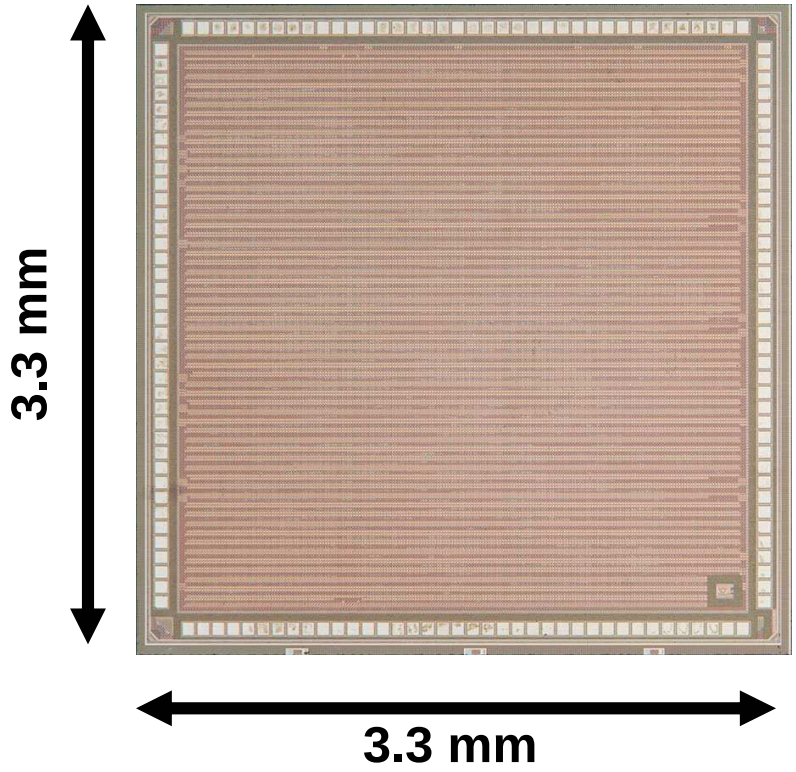


Energy-Area Tradeoff

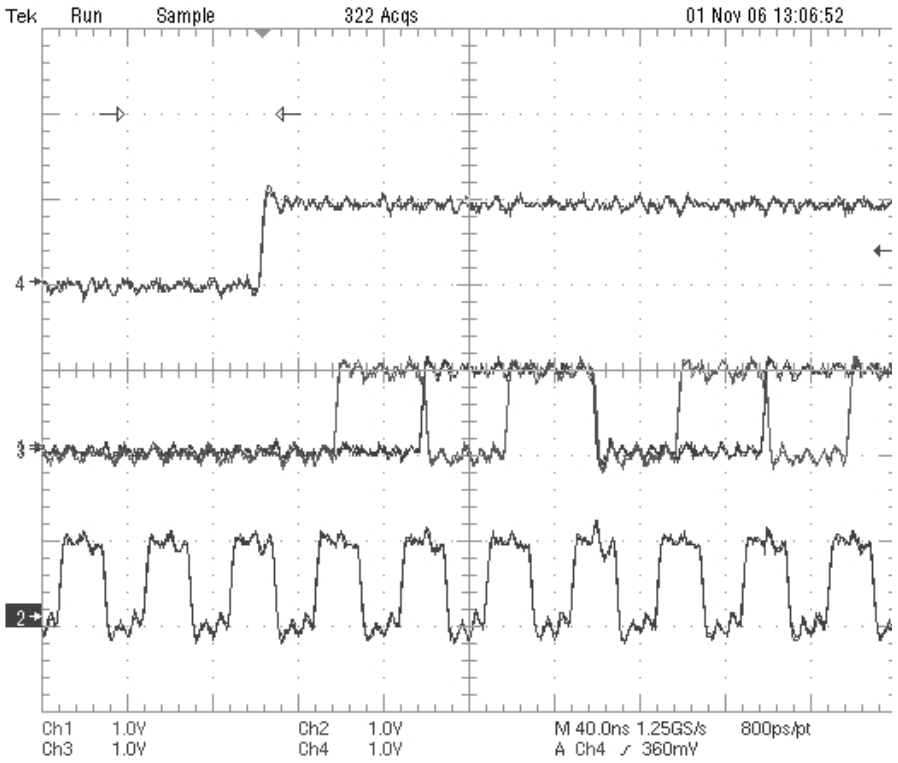


400-mV Baseband Processor

- STMicroelectronics standard-V_T 90-nm CMOS process
- 281,260 gates
- Includes 620 Correlators & 4 Maximum Ratio Combiners
- Die area: 10.94mm^2
  - Active area 23%



Correct Operation at 400 mV



Data Ready

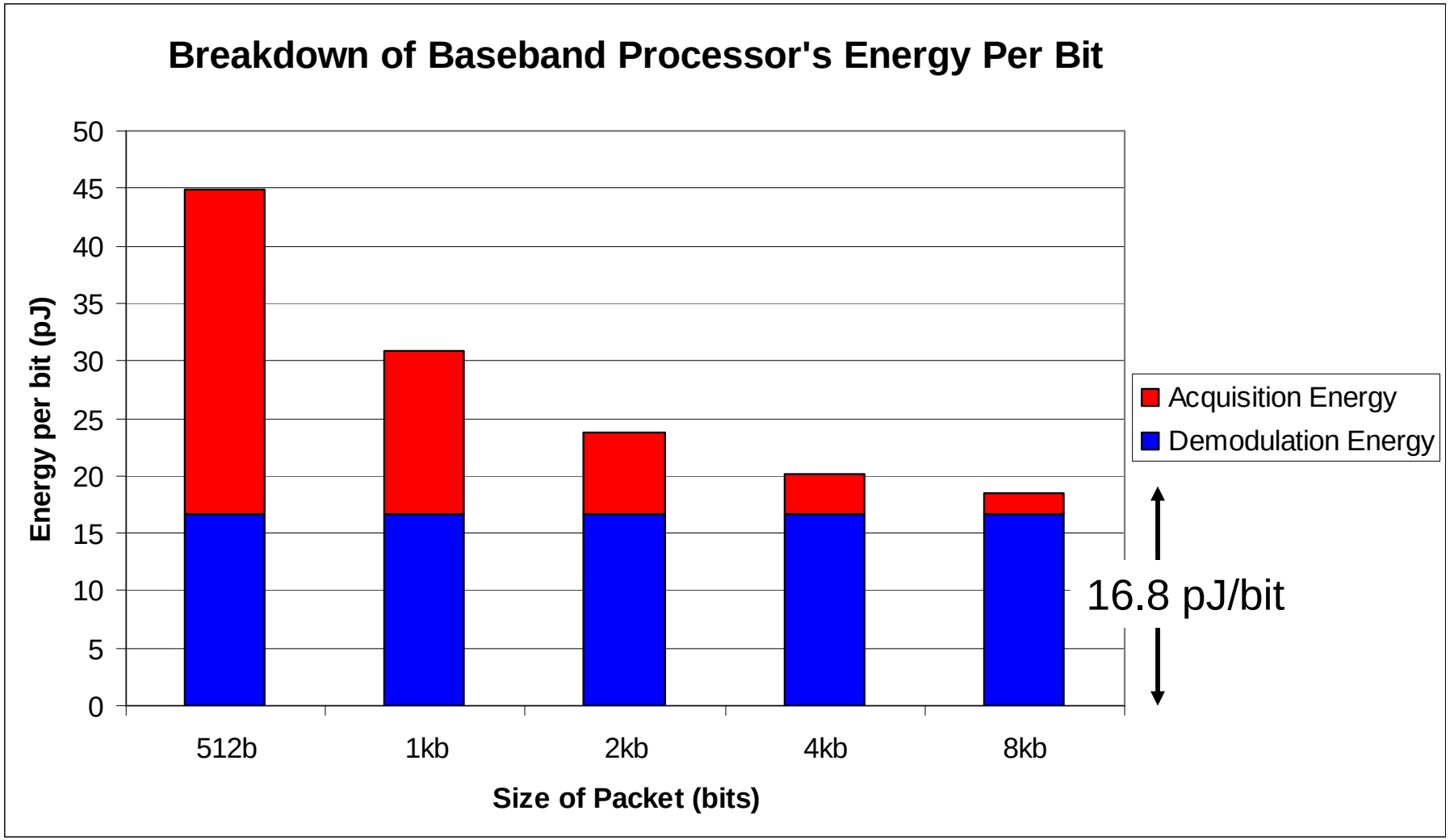
Output Data [1-0]

Output Clock

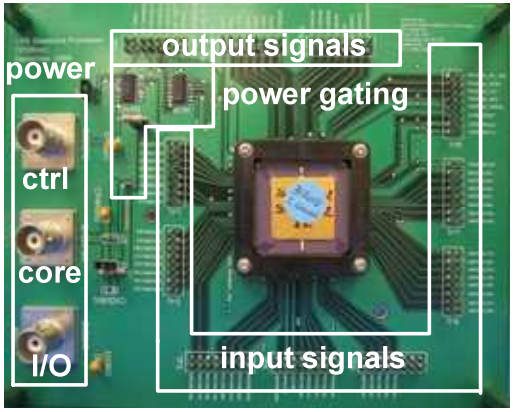
- Oscilloscope plot shows correct functionality at 400mV
  - Note: I/O has a 1V power supply
- Operating frequency of 25 MHz
- Four bits demodulated in parallel every 40-ns cycle

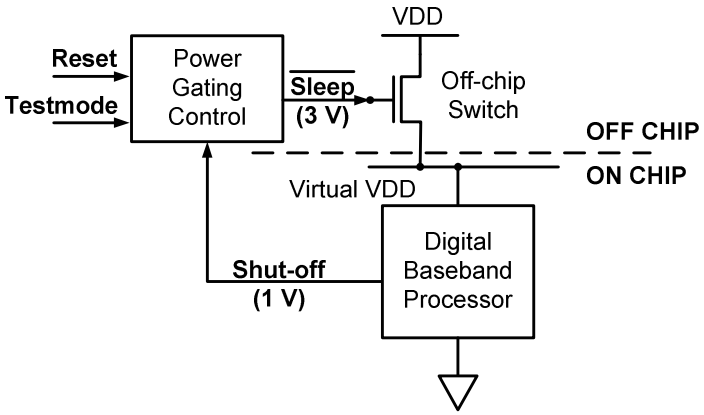
Energy Per Bit

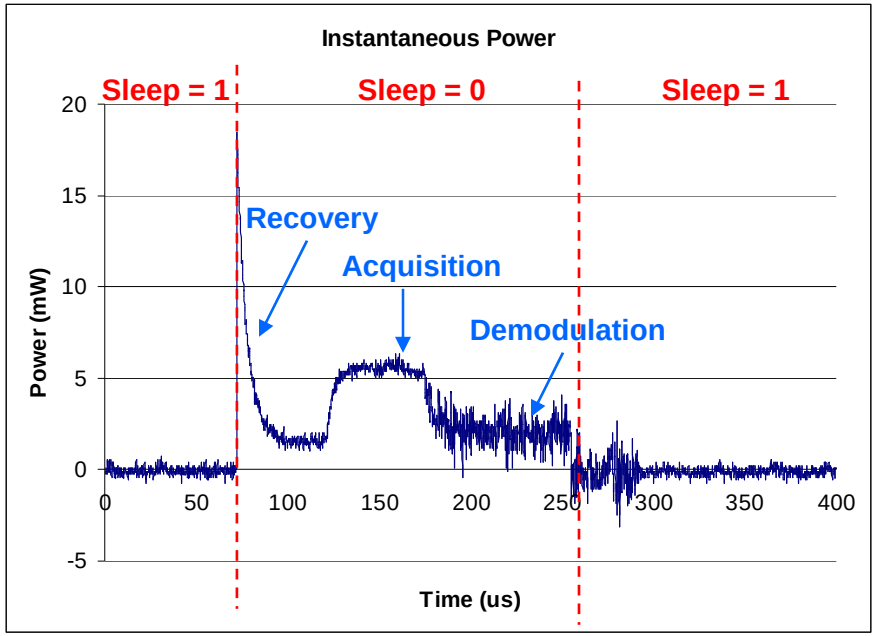
- Power Measurements
  - Acquisition 7 mW / Demodulation 1.7 mW



Power Gating







- Reduce leakage power using a high V_T "sleep" transistor to gate the leakage current when block is idle
- Breakeven time 137 µs

Conclusions

- Reduce energy to receive a UWB packet by
  - Scaling to optimum supply voltage
  - Mapping algorithm to parallel architecture
- Voltage scaling to ultra-low voltage (1 V → 0.4 V)
  - 5.8X reduction in energy per operation of correlators
- Reduced acquisition time
  - 14.7X reduction in receiver acquisition energy
- 400-mV 100 Mbps UWB Baseband Processor
  - 16.8 pJ/bit for demodulation
  - 20 pJ/bit for a 4-kb packet
- Demonstrate high performance at ultra-low voltage
- Can be applied to other high performance communication and signal processing applications

Acknowledgements

- Funding: DARPA and NSERC Fellowship
- Chip Fabrication: STMicroelectronics