A 19pJ/pulse UWB Transmitter with Dual Capacitively-Coupled Digital Power Amplifiers

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***Abstract* — A fully integrated pulsed-UWB transmitter that communicates in the 3-to-5 GHz 802.15.4a bands is presented. Enabled by relaxed frequency tolerances of non-coherent communication, the all-digital architecture generates FCC-compliant UWB pulse-bursts using discrete four-level pulse shaping. BPSK-modulation is achieved without the use of a balun through dual capacitively-coupled digital power amplifiers. The transmitter consumes zero static bias power and achieves an energy efficiency of 113-to-19pJ/pulse at data rates from 100kbps-to-15.6Mbps.**

***Index Terms* — Ultra-wideband, UWB, non-coherent, power amplifier, pulse shaping, transmitter.**

I. Introduction

The demand for increased battery life in consumer, medical, and industrial electronics has emphasized the importance of energy conscious circuit and system design. Since radio components often dominate the power budget of wireless systems, improving the energy efficiency of RF circuits is paramount and has been a key driving force behind the IEEE 802.15.4 and 802.15.4a standards [1].

Due to their inherently duty-cycled nature, pulsed ultra wideband (UWB) architectures have been shown to be amenable to low-power solutions [2,3]. Transmitter signal generators and power amplifiers (PAs), two blocks that typically dominate the power budget of narrowband systems, can be replaced by simple digital pulse generators and CMOS buffers [4]-[8]. Furthermore, non-coherent communication relaxes center frequency tolerances, thus allowing for reduced hardware complexity and enabling the use of highly digital architectures [9,10]. However, low-swing analog modulators, large area baluns, and/or off-chip filters are still often required for BPSK signal generation and FCC-compliant operation.

This paper presents an all-digital pulsed-UWB transmitter in 90nm CMOS, operating in the 3-to-5 GHz UWB band at the three channels specified by the 802.15.4a standard. Digital pulse shaping results in FCC compliance without the use of any off-chip filters. BPSK modulation is achieved without the use of a balun by capacitively combining two signal paths which are in-phase at RF, but have counter-phase common mode components that are cancelled. The all-digital architecture does not require a slow start-up phase locked loop (PLL), and is highly amenable to deeply scaled digital CMOS processes.

II. Transmitter Architecture

A block diagram of the pulsed UWB transmitter is shown in Fig. 1. Payload data is modulated using time-hopped pulse position modulation (TH-PPM), where a PPM symbol is represented by a burst of several back-to-back pulses contained in a fixed window of time [1,8]. In idle mode between bursts, all transmitter circuits are off and the transmitter consumes only leakage power.

Pulse bursts are generated on the rising edge of the offchip *start TX* signal, which enables a digitally controlled oscillator (DCO). The DCO output is modulated and amplified through dual single-ended digital power amplifiers (PAs). The DCO output frequency is calibrated and dynamically adjusted using an early-late detector in a digital frequency-locked loop (FLL).

The DCO output is also synchronously divided to a 499.2MHz clock as specified by the 802.15.4a standard [7]. Several phases of the divided clock are used by pulse shaping circuitry to dynamically shape the PA envelope to one of four discrete levels. The 499.2MHz clock sets the pulse repetition frequency (PRF) within a burst, and is also used in conjunction with a counter to program the number of pulses transmitted per burst.

As the UWB system employs non-coherent modulation, no information is encoded in the phase of the pulse; however, pseudo-random phase modulation is necessary

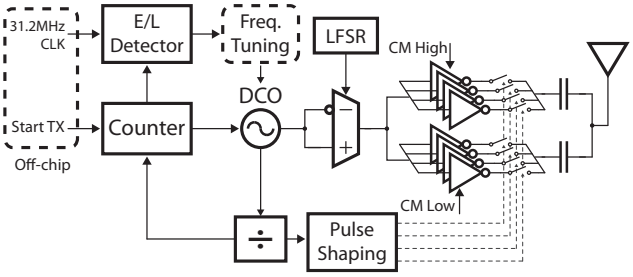

Fig. 1. Transmitter block diagram.

to scramble the output spectrum in order to reduce spectral lines that otherwise limit the total radiated power under FCC limits. BPSK scrambling information is generated by an LFSR at 499.2MHz and applied to a delay-matched single-to-differential multiplexor at the output of the DCO, which drives the dual PAs.

III. Dual Digital Power Amplifiers

A key challenge in pulsed-UWB power amplifier design is how to achieve energy efficiency and spectral compliance while requiring as little chip and circuit board area as possible. Traditional differential analog PAs operating in their linear region can easily achieve spectral compliance, but typically have poor power efficiency [11]. Highly digital PAs can achieve much better power efficiency, but often require off-chip filters or baluns to enable BPSK modulation and/or achieve spectral compliance [5,6,10]. The proposed digital power amplifier achieves both power efficiency and spectral compliance in minimal chip area through two key approaches:

1) Dual capacitively-coupled digital power amplifiers, shown in Fig. 2, allow for the nulling of common-mode components that occur during turn-on and turn-off of the single-ended PAs. This approach does not use any analog circuits and removes the need for an area-expensive balun to interface with a single-ended antenna. Moreover, this approach allows for BPSK modulation to be easily realized.
2) The dual PAs are comprised of several parallel drivers. Digital pulse shaping is achieved by dynamically switching drive strength, resulting in spectrally compliant pulses while minimizing power consumption.

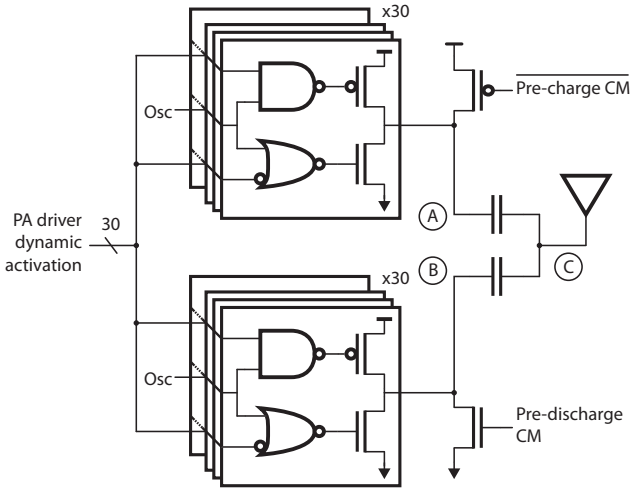

Fig. 2. Dual digital power amplifiers employing capacitively-coupled BPSK signal generation.

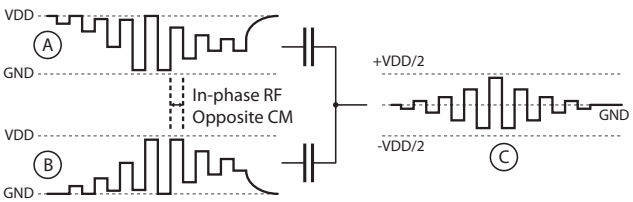

Fig. 3. Capacitive combining timing diagram generating bi-polar RF signals using single-ended digital circuits.

As illustrated in Fig. 3, the single-ended dual digital PAs generate pulses which are in-phase at RF but have counter-phase common mode components. By capacitively combining the two paths, the opposite common modes are cancelled and the zero-DC bi-polar RF signal propagates to the single-ended antenna. The common mode cancellation significantly reduces the low-frequency turn-on and turn-off spurs typically associated with single-ended digital driving circuits. BPSK modulation is achieved by simply inverting the oscillator signal while maintaining opposite common modes on the dual paths. The coupling capacitors also form a first order high-pass filter between the outputs of the PAs and the antenna, thereby further attenuating low frequency out-of-band spectral components.

The dual PAs are each comprised of 30 parallel tri-state inverters. Individual inverters are dynamically enabled and disabled by pulse shaping logic to adjust the PA drive strength through parallel combination. Pre-charge and pre-discharge transistors set the PA output common mode levels to VDD and GND when the PAs are tri-stated between pulses. Since the PA outputs can be tri-stated, the transmitter can share an antenna with a receiver.

IV. Pulse Shaping Logic

A block diagram of the pulse shaping circuitry is shown in Fig. 4. The divider, realized in TSPC logic, produces output clock phases $\Phi_{1\text{-}4}$ with duty cycles of approximately 20%, 40%, 60%, and 80% respectively. The four clock phases are XOR-ed to produce two pulse shaping signals. These two pulse shaping signals are each passed through one-tap FIR filters to increase the number of pulse shaping signals to four. The delay elements of the FIR filters are comprised of a programmable number of inverters.

Each tri-state inverter of the dual PAs is individually programmed through a multiplexor network to receive one of the four pulse shaping signals as a dynamic activation input. For gain control, each inverter can optionally be disabled. Maximum PA output swing is achieved when all four pulse shaping signals are high, i.e. the maximum

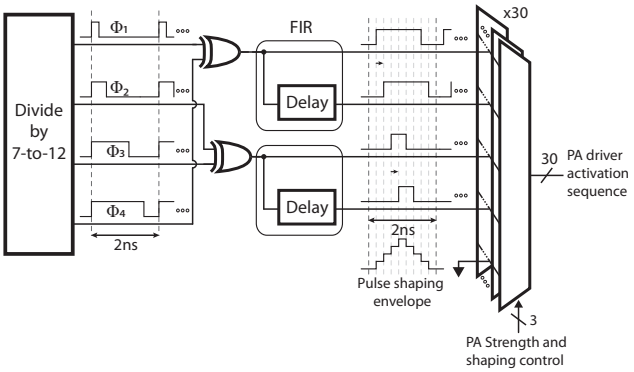

Fig. 4. Four-level pulse shaping circuitry.

number of PA inverters are enabled in parallel simultaneously. Pulse shaping also ensures that the signal amplitude is zero during BPSK phase transitions to avoid common-mode glitching and inter-pulse interference. Programmability is achieved via an on-chip shift register.

V. Digitally Controlled Oscillator

The DCO is a 3-stage current starved ring oscillator, shown in Fig. 5. The highly digital, single-ended structure is designed to have a fast turn-on time on the order of 2ns to reduce energy consumption in duty-cycled operation. Coarse frequency tuning is provided by switchable load capacitors, while fine frequency tuning is provided with NMOS and PMOS current starving DACs.

To simplify the frequency locking algorithm, all three current starving DACs are set to the same digital value, except that the second and third stage DACs can be individually incremented by one for increased resolution. This technique results in a resolution of 7.5 bits from the DACs and 2 bits from the 3 thermometer encoded capacitors, totaling 9.5 bits. As non-coherent signaling does not require precise frequency tolerances, this resolution of frequency control is sufficient to meet receiver sensitivity requirements. The worst-case measured frequency step size in the 3-5 GHz band is 10MHz, corresponding to a PPM accuracy of 2800ppm.

Using the on-chip early-late detector, a SAR algorithm for initial turn-on frequency calibration has been implemented that converges within 12 pulse-bursts, i.e. 0.77μs when operating at 15.6Mbps. Once the DCO has been calibrated, the early-late detector can be used in a low-power frequency-locked loop to dynamically update the current-starving bits for robustness against PVT [7].

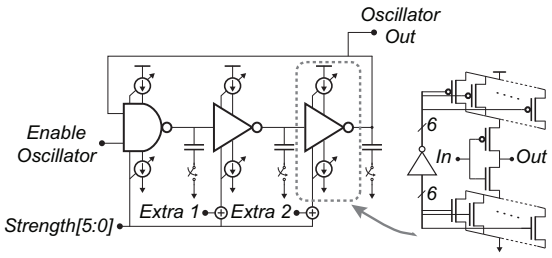

Fig. 5. Digitally controlled oscillator schematic.

VI. Measurement Results

The transmitter was fabricated in 90nm CMOS and operates on a 1V supply. The transmitter and DCO have a core area of 0.07mm^2; a die photo is shown in Fig. 6. Fig. 7 presents a 3.5GHz transient waveform with five pulses concatenated into a single burst. The resulting pulse-bursts achieve both indoor and outdoor FCC compliance in all three bands without requiring the use of an off-chip filter, as shown in Fig. 8. The four-level pulse shaping realizes 15-to-20dB of sidelobe rejection, as illustrated in Fig. 9. The dual digital PAs achieve up to 12dB of low-frequency sidelobe rejection, have a gain scalability of 13dB, and a maximum output swing of 710mV$_{pp}$.

The transmitter consumes 180μW-to-4.8mW (including ESD and I/O supplies) at data rates from 100kbps-to-15.6Mbps. This results in energy efficiencies of 113-to-19pJ/pulse for 16-pulse bursts. Fig. 10 illustrates the energy efficiency of this design compared to recently published works. All measured results were obtained using a 40-pin QFN package.

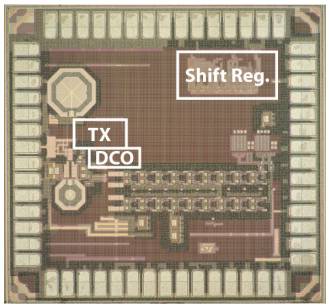

Fig. 6. Transmitter die photograph.

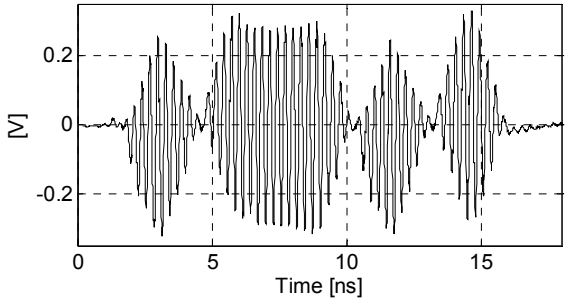

Fig. 7. Measured transient waveform at 3.5GHz with 5 pulses in one burst.

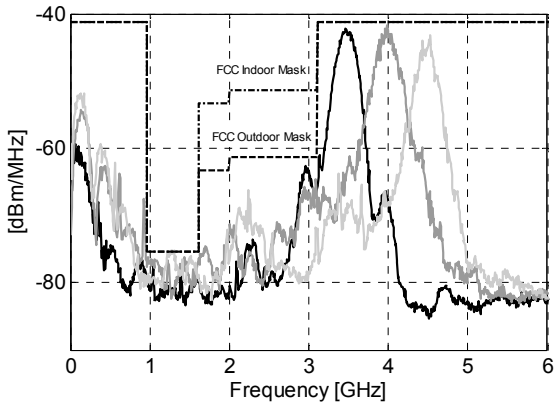

Fig. 8. Measured output spectra of sixteen-pulse bursts.

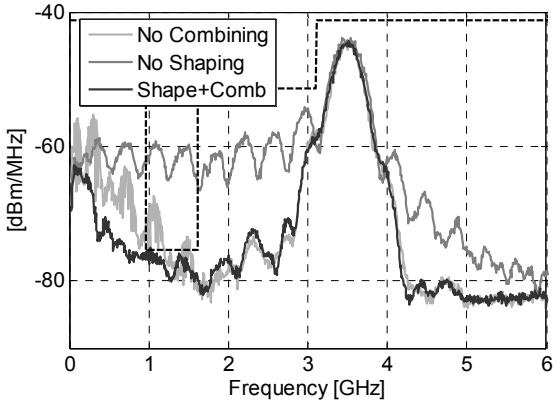

Fig. 9. Output spectra of two-pulse bursts with a) shaping and no combining, b) combining and no shaping, and c) shaping and combining.

VII. Conclusion

An all-digital pulsed-UWB transmitter operating in the 3-to-5GHz UWB band is presented. The transmitter utilizes dual capacitively-coupled digital power amplifiers to enable BPSK modulation without the use of an area-expensive balun. Four-level pulse shaping is employed to achieve both indoor and outdoor FCC compliance without the use of any off-chip filters. A fast start-up single-ended DCO is used in conjunction with an FLL for energy-efficient frequency generation. The all-digital architecture draws zero static bias currents and consumes only switching (CV^2) energy and subthreshold leakage energy. The resulting energy efficiency measures 113-to-19pJ/pulse at data rates from 100kbps-to-15.6Mbps.

Acknowledgements

This work is funded in part by DARPA HI-MEMS (contract FA8650-07-C-7704) and NSERC. Chip fabrication was provided by STMicroelectronics. The authors thank Nathan Ickes for testing support.

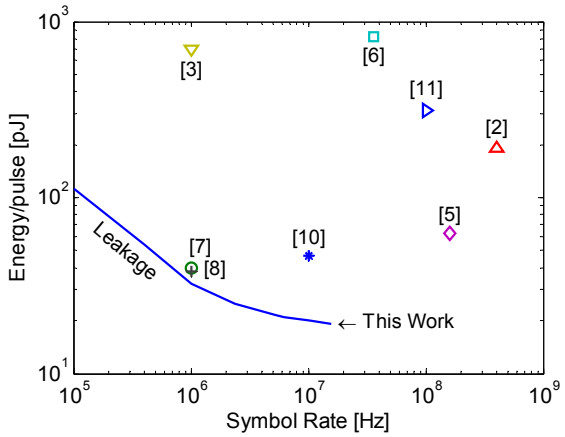

Fig. 10. Energy efficiency of this work compared to previously published results.

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