A high-level drawing of the cyborg moth system is presented in Fig. 11.3.1. Commands are sent from a base station and received wirelessly on a Manduca sexta hawkmoth. A unidirectional wireless link is employed to reduce power consumption of the moth electronics. A tungsten 4-electrode stimulator is implanted in an adult moth to stimulate nervous tissue in the abdominal nerve cord, thereby causing abdominal movement, which has been shown to alter flight direction [1]. A 5MnA, 0.2g Zinc-Air hearing aid battery supplies energy to the system at 1.3V, and is regulated to 1V and 2.5V by an LDO and a dc-dc boost converter. As the carrying capacity of a moth is limited to approximately 0.8g [2], a highly integrated UWB RX SoC is required. Pulsed UWB wireless signaling is employed as UWB radios can achieve highly integrated, energy efficient operation in nanometer CMOS processes.

A block diagram of the RX architecture and packet structure is shown in Fig. 11.3.2. The non-coherent, energy detection RX receives UWB pulses in one of three 500 MHz channels at 3.5, 4.0 and 4.5 GHz. The RX achieves near compliance with 802.15.4a but with minor changes to reduce power consumption. The received signal is amplified by an LNA and multi-stage frequency tunable RF amplifier and then squared to baseband. At baseband, the signal is amplified and then integrated in a 31.2ns window and converted to a 5-bit digital code that represents the total energy received within the integration window. An embedded controller triggers the RX to periodically wake-up from sleep and look for transmitted data. If a packet is detected, the digital synchronizer determines the timing offset between TX and RX to ±1ns accuracy [3]. A 16-phase DLL provides the necessary clock phase to the windowed integrator and ADC to compensate for this offset. The 32MHz system clock is generated by an oscillator and off-chip crystal resonator. Due to the non-coherent RX, no PLL or RF clock is required. Received packets are processed by a PWM controller, which drives the implanted electrodes with 2.5V pulses of programmable width, frequency, and repetition length.

The LNA consists of a common-gate, common-source tuned inverter-based amplifier that realizes single-to-differential conversion, as shown in Fig. 11.3.3. Following the LNA are 5 stages of tuned, differential inverter-based RF amplifiers. To achieve gain scalability up to 35dB, a programmable number of amplifiers can be enabled at any time. To dc bias each inverter, the center tap of each stage’s inductor is connected to the center tap of adjacent stages. As these nodes are virtual grounds this technique does not reduce gain. The inverter-based RF amplifier achieves comparable energy efficiency to low-voltage (0.5V) tuned amplifiers [4] while only requiring half the total number of inductors. Moreover, the higher operating voltage allows for a single core supply voltage of 1V while requiring significantly less current, easing power supply demands. Finally, the inverter-based RF amplifiers allow for simple implementation of a squarer with differential outputs.

Following the RF front end and squarer is a 3-stage baseband amplifier, an integrator and an ADC (Fig. 11.3.4). The entire signal chain from LNA output to ADC input is differential to provide rejection of substrate and power supply noise. The integrator consists of a differential transconductor that discharges multiple nodes from VDD in succession. This pipelined integration approach allows for back-to-back integration windows and provides 2b of coarse ADC quantization. Due to its dynamic structure, the integrator has guaranteed stability and does not require a high-gain op amp. Following the multi-stage differential integrator are single-ended flash ADCs that provide 3b of fine quantization. Compared to a 1b relative compare baseband [4], the 5b of data provided by the integrator and ADC allow for much faster synchronization and support demodulation of on-off keyed (OOK) signals. At the start of each RX packet, a digital calibration loop determines the appropriate baseband amplifier offset current and integrator current to maximize dynamic range and cancel offsets. The static performance of the 5-bit integrator and ADC is shown in Fig. 11.3.4. A DNL of +0.55/-0.62 and an INL of +1.5/-1.6 are achieved.

The RX has been mounted on a miniature, 1.2cm by 2.5cm PCB and has successfully received packets on a moth while battery powered, inducing moth abdominal motion (Fig. 11.3.5). By changing the pulse frequency, the abdominal deflection can be varied between 0° and 7°. The PCB is attached to the moth’s dorsal thorax with glue and mounted like a fin. As the system weight is slightly more than the moth’s carrying capacity, the moth is not able to gain lift; however, when the moth is tethered from a string, normal wing movement and abdominal response to stimulation pulses is observed. In a separate experiment, mock PCBs have been mounted on a moth’s ventral abdomen using a harness and flight has been demonstrated with a 0.8g dummy load. To reduce the system weight below 1g, it is necessary to exploit SiP solutions where the RX SoC is stacked with the microcontroller. The stimulator is inserted ventrally at the junction of the thorax and abdomen while the adult moth is anesthetized with ice. Teflon coated stainless steel wires connect the stimulator with the PCB, looping behind the tip of the abdomen. On power-up, a microcontroller with embedded Flash memory programs the RX through a serial interface and then enters a low-power sleep mode.

The RX SoC was fabricated in a 90nm CMOS process. The RX operates at a 16Mb/s instantaneous data rate and achieves a sensitivity of -76dBm at 10⁻¹² BER, corresponding to a duty cycled sensitivity of -98dBm at 100kb/s. The RX SoC instantaneous power scales from 8-to-22.7mW while demodulating data, yielding 0.5-to-1.4nJ/b. In the cyborg moth system, the duty cycled RX looks for a packet of data every millisecond, requiring an overall average system power of 2.5mW at 1.3V. A table of results is shown in Fig. 11.3.6. A die micrograph is shown in Fig. 11.3.7.

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References:
**Figure 11.3.1:** Cyborg moth motion control system.

**Figure 11.3.2:** Block diagram of pulsed UWB RX SoC and packet structure.

**Figure 11.3.3:** Inverter-based, 6-stage RF front end. Any of the 5 stages following the LNA can be disabled to reduce power consumption.

**Figure 11.3.4:** Integrator/ADC block diagram and DC-input DNL/INL.

**Figure 11.3.5:** Photo of tethered moth before and during stimulus, showing abdominal deflection, with stimulus measured results below.

**Figure 11.3.6:** Table of measured results.

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**System Component** | **Weight**
--- | ---
Packaged RX SoC | 110 mg
1.5 x 2.6 x 0.05 cm PCB | 300 mg
Antenna | 164 mg
Power-Up Programmer | 59 mg
Zinc-Air Battery | 193 mg
Other Components | 174 mg
**TOTAL** | **1000 mg**

**UWB Receiver & System Logic**

Inverter-based, 6-stage RF front end. Any of the 5 stages following the LNA can be disabled to reduce power consumption.

**Transmitter**

**Receiver & Stimulator on Moth**

**Tungsten Electrode Stimulator**

1.95ns UWB Pulses at 3.5 GHz, 4 GHz, or 4.5 GHz

**Transmitter**

**Receiver & System Logic**

**Packet Structure**

**Receiver State**

Detection & Synchronization

Detect

Demodulate

32 repetitions of OOK modulated sync. code

PPM modulated payload

**Packet Structure**

**Receiver State**

Detection & Synchronization

Detect

Demodulate

32 repetitions of OOK modulated sync. code

PPM modulated payload

**Transmitter**

**Receiver & System Logic**

**Digital Logic**

Noncoherent Synchronizer & Demodulator

Cal. Logic

2.5V Moth Stimulator

**Transmitter**

**Receiver & System Logic**

**Digital Logic**

Noncoherent Synchronizer & Demodulator

Cal. Logic

2.5V Moth Stimulator

**Transmitter**

**Receiver & System Logic**

**Digital Logic**

Noncoherent Synchronizer & Demodulator

Cal. Logic

2.5V Moth Stimulator

**Transmitter**

**Receiver & System Logic**

**Digital Logic**

Noncoherent Synchronizer & Demodulator

Cal. Logic

2.5V Moth Stimulator

**Process**

90nm CMOS

**Die Area**

2.6mm × 2.1mm

**Supply voltage**

1V (Core), 2.5V (I/O & Stimulus)

**Modulation**

On-off keying (Preamble), Pulse-position modulation (Payload)

**f_s, sub-bands**

3.5GHz, 4GHz, 4.5GHz

**Receiver PHY Measured Results**

\( f_s = 4.0GHz, \quad T_{th} = 31.25ns \)

**Maximum Sensitivity**

-76dBm at 10³ BER, 16Mb/s

**Front-end NF**

9 dB

**Energy-per-bit**

0.5 nJ/b to 1.4 nJ/b (for complete SoC)

**System Results**

**PCB Area**

1.5cm × 2.6cm

**Total System Weight**

1000mg

**Power Consumption**

2.5mW at 1.3V

**Moth Abdominal Deflection**

Up to 7°
Figure 11.3.7: Die micrograph of pulsed UWB RX SoC.