A 512kb 8T SRAM Macro Operating Down to 0.57V with an AC-Coupled Sense Amplifier and Embedded Data-Retention-Voltage Sensor in 45nm SOI CMOS

Masood Qazi¹, Kevin Stawiasz², Leland Chang², Anantha Chandrakasan¹

¹Massachusetts Institute of Technology
²IBM Thomas J. Watson Research Center

ISSCC 2010
CMOS Voltage Scaling

- **Need**: A memory compatible with the limits of static CMOS logic
- **Solution**: A voltage scalable, single-supply, 8T SRAM with no dynamic assists that minimizes area and standby power
Features of This Work

- AC-Coupled Sense Amplifier (ACSA)
- Regenerative Global Bitline Scheme
- Data-Retention-Voltage Sensor
Sensing Approaches

CONVENTIONAL TECHNIQUES

128 to 256 ROWS

THIS WORK

small swing
Sensing Approaches

CONVENTIONAL TECHNIQUES
128 to 256 ROWS

THIS WORK
128 to 512 ROWS

small swing

full swing
Sensing Approaches

CONVENTIONAL TECHNIQUES
128 to 256 ROWS

128 to 512 ROWS

THIS WORK
4096 ROWS

small swing

full swing

8T cell

small swing
AC Coupled Sense Amplifier (ACSA)
AC Coupled Sense Amplifier (ACSA)
AC Coupled Sense Amplifier (ACSA)

8T bitcell

Sensing PMOS

Dynamic output

C_L ~ 2fF
AC Coupled Sense Amplifier (ACSA)

8T bitcell

Thick oxide MOS capacitor

Sensing PMOS

Dynamic output

$|V_{Tp}|$
AC Coupled Sense Amplifier (ACSA)

8T bitcell

Thick oxide MOS capacitor

Equalize PMOS

Sensing PMOS

Dynamic output

$C_L \sim 2fF$
AC Coupled Sense Amplifier (ACSA)

8T bitcell

RWL

Q

M1

M2

256

LBL

ϕ

+|V_Tp|

Thick oxide MOS capacitor

Equalize PMOS

Sensing PMOS

Amplifying PMOS

Dynamic output

C_L ~ 2fF
AC Coupled Sense Amplifier (ACSA)

8T bitcell

Thick oxide MOS capacitor

Equalize PMOS

Sensing PMOS

GBL positive feedback (discussed later)

Amplifying PMOS

Bias pull-down

Dynamic output

$C_L \sim 2fF$
ACSA Operation

Sense “1” Sense “0”

![Diagram of ACSA Operation](image-url)
ACSA Output Current

Steep cutoff of PMOS stack M3-M4 distinguishes “1” and “0”
Offset Compensation Reduces Delay

Simplified schematic during evaluation

\[ I_{\text{out}} = f(V_{SG4} - |V_{Tp}| + \Delta V_T) \]

\[ I_{\text{out}} = f\left( |\Delta V_{LBL}| - \frac{|V_{Tp}| + \Delta V_T}{1 + g_{m3}r_o} \right) \]

Amplification by M3 suppresses variation

![Voltage Waveforms](image)

- **RWL**
- **Proposed**
- **Conventional**

SS corner 25°C

5σ delay 1.8x slower
Offset Compensation Lowers $V_{MIN}$

Variation in sensing network is critical to $V_{MIN}$
Regenerative Global Bitline Scheme
Regenerative Global Bitline Scheme

1 of 8 Banks

* For testability, separate write path (not shown) is implemented.
Die Photo and Area of Sensing Network

On-chip data compare and failcount generation

Data input, control, and address repeaters

read circuits, one col.

write driver coupling cap
Measured Read Access Time

Bank7 (512 rows)

Bank0 (512 rows)

Clock Buffering

ACLK

CLK

GBL

1.7mm
The two measurements below 0.65V require partial turn-on of a bleeder PMOS.
Data Retention and Standby Power

Knowing the limit of the data-retention-voltage (DRV) enables dramatic reduction of standby power.
Current Approaches to the DRV

Conventional approaches cannot track global variation and require separate knowledge of the DRV.
Tracking the DRV

The DRV is a function of process corner and temperature.

**Replica Cell Biasing**

[Takeyama et al. 2005 VLSI]

Bias Array voltage to:

\[ VDD - VSS = 2 \times V_T \]

**Canary Replica**

[Wang et al. 2007 CICC]

Calibrate against known DRV distribution.

Key challenge: Predict the DRV on-chip while preserving the state of the memory and the array efficiency of the design.
# $5\sigma$ Measurement with $2\sigma$ Sampling

<table>
<thead>
<tr>
<th>Simulation Realm</th>
<th>General method, Easy to implement</th>
<th>Efficient utilization of resources</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Monte Carlo:</td>
<td>Importance Sampling &amp; worst-case point:</td>
</tr>
<tr>
<td></td>
<td>$N_{MC} = 100/p$</td>
<td><img src="image" alt="Diagram" /></td>
</tr>
<tr>
<td></td>
<td>$p \sim 10^{-5}$ to $10^{-7}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$N \sim 10^7$ to $10^9$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>[N. Metropolis and S. Ulam 1949]</td>
<td></td>
</tr>
<tr>
<td>Hardware Realm</td>
<td>Yield learning vehicle</td>
<td>?</td>
</tr>
</tbody>
</table>

[Antreich et al. 1991 ICCAD, Dolecek et al. 2008 ICCAD, Qazi et al. 2010 DATE]
# 5σ Measurement with 2σ Sampling

<table>
<thead>
<tr>
<th>Simulation Realm</th>
<th>General method, Easy to implement</th>
<th>Efficient utilization of resources</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Monte Carlo:</td>
<td>Importance Sampling &amp; worst-case point:</td>
</tr>
<tr>
<td></td>
<td>(N_{\text{MC}} = 100/\rho)</td>
<td>[Antreich et al. 1991 ICCAD, Dolecek et al. 2008 ICCAD, Qazi et al. 2010 DATE]</td>
</tr>
<tr>
<td></td>
<td>(\rho \sim 10^{-5} \text{ to } 10^{-7})</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(N \sim 10^{7} \text{ to } 10^{9})</td>
<td></td>
</tr>
<tr>
<td></td>
<td>[N. Metropolis and S. Ulam 1949]</td>
<td></td>
</tr>
</tbody>
</table>

| Hardware Realm  | Yield learning vehicle             | THIS WORK                         |
The DRV Sensor Overview

- Single column of 256 memory cells for each 32kb half-bank
- < 2% area overhead
- Split supply wiring
- Independent programming path
- Recover functional relation between $V_T$ and SNM

$$SNM(\Delta V_T) = 1 + c_1 \Delta V_{T1} + c_2 \Delta V_{T2} + c_3 \Delta V_{T3} + c_4 \Delta V_{T4} + c_5 \Delta V_{T5} + c_6 \Delta V_{T6}$$
Identical layout of sensor cell transistors will track RDF mismatch

*2T read stack not shown for clarity.
Skew on Supply Emulates $V_T$ Shift

Example supply skew ($Q = \text{"0"}$):

\[ \Delta V_{Teff}^T = \begin{bmatrix} -100mV & 100mV & 100mV & 0 & 0 & -100mV \end{bmatrix} \]

Effective threshold shift achieved by degenerating VGS
The DRV Sensor Algorithm

Given $\sigma_{vt}$

Select first of three skew directions

Program DRV sensor cells to “0”

Lower to VDDAR to VDDx

Apply and remove voltage skew

Raise VDDAR to full VDD level

Adjust magnitude of skew towards 50% failure rate

Read DRV cells and check for 50% fail Rate (flip to 1)

Record magnitude of current skew and check if all three skews have been obtained

Yes

Select next skew

No

Solve linear system to obtain SNM coefficients and evaluate Pf

Yes

No
The DRV Sensor Algorithm

Given $\sigma_{vt}$

Select first of three skew directions

Program DRV sensor cells to “0”

Lower to VDDAR to VDDx

Apply and remove voltage skew

Raise VDDAR to full VDD level

Adjust magnitude of skew towards 50% failure rate

Read DRV cells and check for 50% fail rate (flip to 1)

Yes

Record magnitude of current skew and check if all three skews have been obtained

Yes

Solve linear system to obtain SNM coefficients and evaluate Pf

No

Select next skew

No

$V_1^{1T} = \frac{k}{\sqrt{2}} \begin{bmatrix} 0 & 1 & 0 & -1 \end{bmatrix}$

$V_2^{2T} = k \begin{bmatrix} 0 & 1 & 0 & 0 \end{bmatrix}$

$V_3^{3T} = k \begin{bmatrix} 0 & 0 & 1 & 0 \end{bmatrix}$

*SNM equation appropriately simplified to 3 degrees of freedom.
The DRV Sensor Algorithm

Given $\sigma_{Vt}$

- Select first of three skew directions
- Program DRV sensor cells to “0”
- Lower to VDDAR to VDDx
- Apply and remove voltage skew
- Raise VDDAR to full VDD level

Adjust magnitude of skew towards 50% failure rate

- Read DRV cells and check for 50% fail Rate (flip to 1)
- Yes
  - Record magnitude of current skew and check if all three skews have been obtained
  - Yes
    - Solve linear system to obtain SNM coefficients and evaluate Pf
  - No
    - Select next skew

- No
  - No
    - Select next skew
  - Yes
    - Solve linear system to obtain SNM coefficients and evaluate Pf
The DRV Sensor Algorithm

Given $\sigma_{Vt}$

Select first of three skew directions

Program DRV sensor cells to “0”

Raise VDDAR to full VDD level

Apply and remove voltage skew

Lower to VDDAR to VDDx

Adjust magnitude of skew towards 50% failure rate

Read DRV cells and check for 50% fail Rate (flip to 1)

Yes

Record magnitude of current skew and check if all three skews have been obtained

Yes

Solve linear system to obtain SNM coefficients and evaluate Pf

No

Select next skew

Example VDDx = 0.4V

0.4V

BLT

M5

M1

“1”

0V

0.4V

BLC

M6

M2

“0”

0V

M4

M3

0V

Yes

No
The DRV Sensor Algorithm

- **Given $\sigma_{Vt}$**
- **Select first of three skew directions**
- **Program DRV sensor cells to “0”**
- **Lower to VDDAR to VDDx**
- **Apply and remove voltage skew**
- **Raise VDDAR to full VDD level**
  - **Adjust magnitude of skew towards 50% failure rate**
  - **Read DRV cells and check for 50% fail Rate (flip to 1)**
    - **Yes**
      - **Record magnitude of current skew and check if all three skews have been obtained**
      - **Yes**
        - **Solve linear system to obtain SNM coefficients and evaluate Pf**
    - **No**
      - **Select next skew**

**Diagram:**
- 0.4V
- 0.3V
- 0.4V
- 0.4V
- 0V
- 0V
- 0V
- 0V
- M1 M2
- M3 M4
- M5 M6
- BLT
- BLC
- “1”
- “0”

- 0.1V
- M5 M6
- BLT
- BLC

- Q
- Q

- M1
- M2
- M3
- M4
- M5
- M6

- BLT
- BLC
The DRV Sensor Algorithm

Given $\sigma_{vt}$

- Select first of three skew directions
- Program DRV sensor cells to “0”
- Lower to VDDAR to VDDx
- Apply and remove voltage skew
- Raise VDDAR to full VDD level
- Adjust magnitude of skew towards 50% failure rate

No

Select next skew

Yes

Read DRV cells and check for 50% fail Rate (flip to 1)

Yes

Record magnitude of current skew and check if all three skews have been obtained

Yes

Solve linear system to obtain SNM coefficients and evaluate Pf
The DRV Sensor Algorithm

- Given $\sigma_{Vt}$
- Select first of three skew directions
- Program DRV sensor cells to “0”
- Lower to VDDAR to VDDx
- Apply and remove voltage skew
- Raise VDDAR to full VDD level
- Adjust magnitude of skew towards 50% failure rate
- Read DRV cells and check for 50% fail Rate (flip to 1)
  - Yes: Record magnitude of current skew and check if all three skews have been obtained
  - No: Select next skew
- Solve linear system to obtain SNM coefficients and evaluate $P_f$

SNM = $1 + [c_1 \ c_2 \ c_4] R T_{0\to1} [V^1 \ V^2 \ V^3] = 0$

$P_f = \phi \left( -\frac{1}{\sqrt{(c_1\sigma_2)^2 + (c_2\sigma_2)^2 + \cdots + (c_6\sigma_6)^2}} \right)$
The spherically symmetric sampling of $V_T$ mismatch enables the insertion of margin.
# 512kb Macro Summary

<table>
<thead>
<tr>
<th>Organization</th>
<th>4096 words x 128b (in 8 banks of 64kb)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>45nm High-Performance SOI</td>
</tr>
<tr>
<td>Cell area</td>
<td>0.578(\text{um}^2)</td>
</tr>
<tr>
<td>Sense Circuit Area Supporting 512b</td>
<td>20.9(\text{um}^2)</td>
</tr>
<tr>
<td>Access time at 1.2V</td>
<td>400ps</td>
</tr>
<tr>
<td>Access time at 0.57V</td>
<td>3.4ns</td>
</tr>
<tr>
<td>Active Power at 1.2V (extrapolated from 100MHz to 1.25GHz)</td>
<td>169mW</td>
</tr>
<tr>
<td>Leakage Power at 1.2V</td>
<td>338mW</td>
</tr>
</tbody>
</table>

![Diagram of row decoder and 64kb Bank]
Conclusions

• AC-coupling is viable on a finer scale in advanced CMOS technology.
• Variation-tolerant sensing networks are needed to operate closer to the fundamental voltage scaling limits of the bitcell.
• Statistical fluctuation can be predicted on-chip by recovering the functional relation between variation parameter and performance metric.

Acknowledgement: FCRP Focus Center for Circuit & System Solutions (C2S2) for funding.