A Resolution-Reconfigurable 5-to-10b 0.4-to-1V Power Scalable SAR ADC

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Motivation for Scalable ADC

- Bio-potentials vary in bandwidth and dynamic range
- DSP algorithms have varying resolution requirements

<table>
<thead>
<tr>
<th>Bio-potential</th>
<th>Bandwidth</th>
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<tbody>
<tr>
<td>EEG (electroencephalography)</td>
<td>0.5 to 40 Hz</td>
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<tr>
<td>ECG (electrocardiography)</td>
<td>0.05 to 100 Hz</td>
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<tr>
<td>EMG (electromyography)</td>
<td>20 Hz to 2 kHz</td>
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Energy-efficient, scalable and reconfigurable ADC is beneficial
Power Scalable SAR ADC

ADC specifications:

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<th>Resolution</th>
<th>5b to 10b</th>
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![Diagram of Power Scalable SAR ADC](image)
Power Scalable SAR ADC

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![Diagram of Power Scalable SAR ADC]

- **C_c**: Capacitors for power scalable ADC
- **4b Sub DAC**: 4-bit sub DAC
- **1-6b Main DAC**: 1-6-bit main DAC
- **Dynamic Comparator**: Compares input with DAC output
- **Resolution Scaling Logic**: Adjusts resolution based on input
- **SAR Logic**: Successive Approximation Register
- **Sample Rate Scaling Logic**: Modulates sample rate
- **Boost**: Increases signal for higher precision
- **High-V_T**: High-threshold voltage
- **Leakage Power-Gating**: Reduces leakage current
- **Clock Gate Logic**: Controls clock signals
- **V_DD**: Supply voltage
- **VIN_DIFF**: Input voltage difference
- **SLEEP**: Clock gating to save power
- **CLK**: Clock signal
Power Scalable SAR ADC

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Diagram showing the components of the SAR ADC.
Power Scalable SAR ADC

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Resolution-Reconfigurable DAC

Leakage Power-Gating
Outline

- Reconfigurable DAC Architecture
- Voltage Scaling
- Leakage Power-Gating
- Measured Results
- Conclusion
Review: Sub-DAC

Conventional Binary-Weighted Array → Large MSB to LSB ratio

Main-DAC/Sub-DAC Array → Reduces ratio, saves area/power

\[ V_{\text{REF}} \rightarrow \begin{array}{c}
2^9C_0 \quad 2^8C_0 \quad 2^7C_0 \quad 2^6C_0 \quad 2^5C_0 \quad 2^4C_0 \quad 2^3C_0 \quad 2^2C_0 \quad 2C_0 \quad C_0 \\
\end{array} \rightarrow V_{\text{OUT}} \]

\[ V_{\text{REF}} \rightarrow \begin{array}{c}
2^4C_0 \quad 2^3C_0 \quad 2^2C_0 \quad 2C_0 \quad C_0 \\
\end{array} \rightarrow V_{\text{OUT}} \]

Main-DAC

\[ C_C = \frac{32}{31}C_0 \]

Sub-DAC

\[ C_0 \]
**Review: Split-Capacitor Array**

*Example: $V_{REF} = 1V$, $V_{IN} = 0.4V$*

Conventional DAC

\[ V_{DAC} = 0.5V_{REF} \]

Split-Capacitor DAC

\[ V_{DAC} = 0.5V_{REF} \]

**Bit Cycle 1 (Up)**

\[ E_{U,CONV,1} = E_{U,SPLIT,1} = 2C_0V_{REF}^2 \]

Up transitions require the same energy for both arrays
Review: Split-Capacitor Array

Example: $V_{REF} = 1V$, $V_{IN} = 0.4V$

**Conventional DAC**

$V_{DAC} = 0.25V_{REF}$

**Bit Cycle 2 (Down)**

$E_{D,CONV,2} = \frac{5}{2} C_0 V_{REF}^2$

**Split-Capacitor DAC**

[B. Ginsburg, ISCAS’05]

$V_{DAC} = 0.25V_{REF}$

$E_{D,SPLIT,2} = \frac{1}{2} C_0 V_{REF}^2$

*Split-Capacitor approach avoids charging capacitors to $V_{REF}$ during down transitions*
Split-Capacitor Array DAC with Sub-DAC

Split MSB capacitor into the MSB Sub-Array, identical in structure to the Main Array.
Split-Capacitor Array DAC with Sub-DAC

MSB Sub-Array (5b Main-DAC/4b Sub-DAC)

Main Array (5b Main-DAC/4b Sub-DAC)
10b DAC Switching Energy

10b Conv. Array (Binary Weighted) Avg: 682

10b Split Capacitor Array Avg: 426

Using Sub-DACs

Conventional (5b Main, 5b Sub) Avg: 41

Split (5b Main, 4b Sub in both arrays) Avg: 34
Adding Reconfigurability

- No power reduction by truncation of bits
- Resolution scaling:
  1. Start at MSB $\rightarrow$ power consumption

![Circuit Diagram]

$V_{REF}$ $V_{OUT}$

- No power reduction by truncation of bits
- Resolution scaling:
  1. Start at MSB $\rightarrow$ power consumption

![Circuit Diagram]

$V_{REF}$ $V_{OUT}$
Adding Reconfigurability

- No power reduction by truncation of bits
- Resolution scaling:
  1. Start at MSB $\rightarrow$ power consumption
  2. Cycle through to LSB $\rightarrow$ attenuation of DAC output
Reconfigurable DAC

- Interleave **MSB Sub-Array** with **Main Array**
- Insert switches to decouple capacitors as resolution is scaled
Reconfigurable DAC – 8b Mode

<table>
<thead>
<tr>
<th>R[4:0]</th>
<th>00111</th>
</tr>
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<tr>
<td>DAC Configuration</td>
<td>4b Main-DAC, 4b Sub-DAC</td>
</tr>
<tr>
<td>MSB Sub-Array</td>
<td>Split 8C₀ (in red)</td>
</tr>
</tbody>
</table>
Differential DAC Schematic

- **MSB Sub-Array**
- **Main Array**

**Top plate sampling switches**

**Interleaved main-DACs**

**sub-DAC**
# Voltage Scaling


\[ E_{ADC} \approx E_{DAC} + E_{COMP} + E_{DIG} + E_{LEAK} \]

<table>
<thead>
<tr>
<th>Block</th>
<th>Energy/Conversion</th>
<th>Voltage Dependence</th>
</tr>
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<tbody>
<tr>
<td>DAC*</td>
<td>( C_{DAC}(2^N, V_{IN}) \cdot V_{DD}^2 )</td>
<td>( V_{DD}^2 )</td>
</tr>
<tr>
<td>Comparator</td>
<td>( N \cdot C_L \cdot V_{DD}^2 )</td>
<td>( V_{DD}^2 )</td>
</tr>
<tr>
<td>Digital</td>
<td>( C_{EFF}(N, V_{IN}) \cdot V_{DD}^2 )</td>
<td>( V_{DD}^2 )</td>
</tr>
<tr>
<td>Leakage**</td>
<td>( V_{DD} \cdot I_{LEAK} \cdot T_s )</td>
<td>( V_{DD} \cdot e^{kV_{DD}} )</td>
</tr>
</tbody>
</table>

* \( V_{REF} = V_{DD} \)

** \( I_{LEAK} \) is exponential with \( V_{DD} \) due to DIBL

**ADC Energy-Per-Conversion benefits from voltage scaling**
Voltage Scaling and Linearity

- Linearity requirements decrease with resolution
Voltage Scaling and Noise

- Noise requirements decrease with resolution

*Leverage voltage scaling with resolution for $CV^2$ savings*
Regenerative Comparator

- 4-bit switched capacitors for 3-σ offset compensation
- Noise degrades ENOB by 1b at 0.5V in 10b mode
Minimum Energy Point

\[ E/\text{conversion} \sim C_{\text{EFF}} V_{\text{DD}}^2 + V_{\text{DD}} I_{\text{LEAK}} T_S \]

- Minimum conversion time \((T_S)\) can be limited by:
  - Sampling bandwidth, reference settling, comparator

[Graph showing energy-per-conversion vs. supply voltage

Minimum energy point

[A. Wang, JSSC’05]
Leakage Reduction

- **SLEEP** mode enables sample rate scaling
- Leakage power-gating applied during **SLEEP**
**Power Gating Break-Even Point**

- **Energy overhead:**
  - Switching gate capacitance: \( E_{SW} = C_G V_{DD}^2 \)
  - Recovery of virtual ground: \( E_{REC} = C_X V_{DD} \Delta V \)

**Require:** \( E_{REC} + E_{SW} < (P_{\text{leak-active}} - P_{\text{leak-sleep}}) T_{\text{sleep}} \)

---

**Do not Power Gate**

**Power Gate**

![Diagram showing power gating logic](image)
ADC Prototype

65nm Low-Leakage Digital CMOS
Measured INL and DNL
\((V_{DD}=0.6V, f_s=100kS/s)\)

5b Mode

\[+0.11\text{LSB}/-0.01\text{LSB}\]

8b Mode

\[+0.51\text{LSB}/-0.07\text{LSB}\]

10b Mode

\[+0.58\text{LSB}/-0.11\text{LSB}\]
Measured FFT

5b Mode
V_{DD}=0.5V
f_S=60kS/s

8b Mode
V_{DD}=0.55V
f_S=20kS/s

10b Mode
V_{DD}=0.55V
f_S=20kS/s

f_{IN}=29.289kHz
SNDR=30dB
SFDR=44dB

f_{IN}=9.763kHz
SNDR=47dB
SFDR=61dB

f_{IN}=9.763kHz
SNDR=55dB
SFDR=69dB
**Measured ENOB**

**ENOB vs Input Frequency**

- **$f_S=1$ MS/s**
- **$V_{DD}=1$ V

- **$f_S=80$ kS/s**
- **$V_{DD}=0.55$ V
Measured Resolution and Voltage Scaling Results

\[ FOM = \frac{P}{2f_{IN} \cdot 2^{\text{ENOB}}} \]

Resolution scaled by truncating 10b data

\( f_S = 200kS/s \)
Measured Resolution and Voltage Scaling Results

- Fixed DAC, Constant $V_{DD}=1V$
- Resolution Scaling, Constant $V_{DD}=1V$

1.7X reduction from DAC scaling

Resolution scaled by truncating 10b data

$f_S=200\text{kS/s}$
Measured Resolution and Voltage Scaling Results

- Fixed DAC, Constant $V_{DD}=1V$
- Resolution Scaling, Constant $V_{DD}=1V$
- Resolution and Voltage Scaling

1.7X reduction from DAC scaling
5X reduction from DAC + voltage scaling
Resolution scaled by truncating 10b data

$f_S=200\text{kS/s}$
Optimum Efficiency Point

Graphs showing the relationship between Supply Voltage [V] and Energy-Per-Conversion [pJ], Max. Sampling Frequency [Hz], and FOM [J/conversion-step] for 5b mode, 8b mode, and 10b mode.
Optimum Efficiency Point

CV^2 losses
Optimum Efficiency Point

CV² losses

Increased conversion time
Optimum Efficiency Point

- **CV^2 losses**
- **Max. Sampling Frequency [Hz]**
- **Energy-Per-Conversion [pJ]**
- **FOM [J/conversion-step]**

- **Increased conversion time**
- **Optimum FOM**
Leakage power dominates below 2kS/s.

Leakage power-gating reduces total power by up to 14% at low frequencies.
# ADC Performance Summary

<table>
<thead>
<tr>
<th>Active Die Area</th>
<th>0.212 mm² (65nm low-leakage CMOS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage ($V_{DD}$)</td>
<td>0.4V to 1V (differential input range is $\pm V_{DD}$)</td>
</tr>
</tbody>
</table>
| Maximum Sampling Rate (all resolutions) | 5kS/s @ 0.4V  
2MS/s @ 1V |
| Resolution Mode                  | 5b  | 6b  | 7b  | 8b  | 9b  | 10b |
| INL [LSB] @ 0.6V, 100kS/s        | 0.07 | 0.33 | 0.33 | 0.43 | 0.50 | 0.57 |
| DNL [LSB] @ 0.6V, 100kS/s        | 0.11 | 0.35 | 0.40 | 0.51 | 0.55 | 0.58 |
| Dynamic Performance @ 0.55V, 20kS/s (*except for 5b data @ 0.5V, 60kS/s) |    |    |    |    |    |    |
| SFDR [dB] @ Nyquist              | *44.0 | 48.5 | 54.6 | 61.2 | 63.0 | 68.8 |
| SNDR [dB] @ Nyquist              | *30.4 | 36.6 | 41.5 | 47.0 | 51.2 | 55.0 |
| ENOB                             | *4.77 | 5.79 | 6.60 | 7.51 | 8.21 | 8.84 |
| Power Consumption [nW]           | *234 | 116 | 133 | 146 | 159 | 206 |

10 samples tested
Comparison with State-of-the-Art

Data courtesy of B. Murmann, “ADC Performance Survey 1997-2010, [Online]”. 

22.4 fJ/conv-step @ 10b
Conclusion

- Power scalable SAR ADC with reconfigurable resolution (5 to 10b)
  - DAC resolution scaling
  - Voltage scaling
- Leakage power-gating important at low sample rates
- Energy-efficient over wide range of resolutions and sample rates

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