Self-Powered Signal Processing Using Vibration-Based Power Generation

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***Abstract*— Low power design trends raise the possibility of using ambient energy to power future digital systems. A chip has been designed and tested to demonstrate the feasibility of operating a digital system from power generated by vibrations in its environment. A moving coil electromagnetic transducer was used as a power generator. Calculations show that power on the order of 400 μW can be generated. The test chip integrates an ultra-low power controller to regulate the generator voltage using delay feedback techniques, and a low power subband filter DSP load circuit. Tests verify 500 kHz self-powered operation of the subband filter, a level of performance suitable for sensor applications. The entire system, including the DSP load, consumes 18 μW of power. The chip is implemented in a standard 0.8 μm CMOS process. A single generator excitation produced 23 ms of valid DSP operation at a 500 kHz clock frequency, corresponding to 11 700 cycles.**

***Index Terms*—DC/DC conversion, low power, self-powered.**

I. Introduction

THERE has been much interest in recent years in low power very large scale integration (VLSI) design stemming from the demands of long battery life in portable systems and heat removal in larger, nonportable ones. Voltage scaling coupled with other algorithmic and architectural optimizations have allowed dramatic scaling of power consumption for a wide variety of low to medium throughput DSP applications [1]. Fig. 1 shows the current power consumption for a variety of such DSP's, including programmable [2], custom [3], and sensor related systems [4], [5]. Projecting current power scaling trends into the future (based on deep voltage scaling and other power management techniques), we expect the power consumption to be reduced to tens of μW to hundreds of μW. At these low power levels, an interesting question arises: can we use ambient energy sources to power electronic systems? Ambient energy is energy that is in the environment of the system and is not stored explicitly, for example, in a battery. Portable systems that depend on batteries have a limited operating life and can fail at inconvenient times, while a circuit powered by ambient sources has a potentially infinite lifetime. In long-lived systems where battery replacement is difficult, generating power from ambient sources becomes imperative. For example, in a smart structure where sensors and actuators are embedded in a bulk material to modify its properties, access to the electronics is greatly reduced.

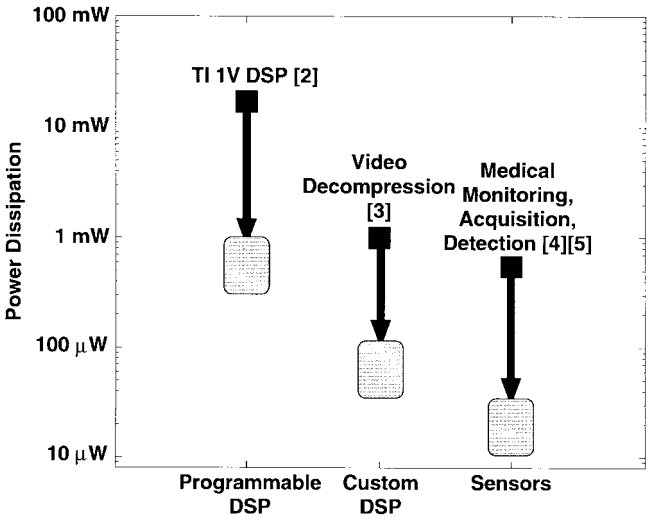

Fig. 1. Trends in power consumption for low to medium throughput DSP.

In this paper, we explore the feasibility of operating a DSP system on power generated by external means. Since ambient energy sources are by definition uncontrolled, we require a mechanism for converting the energy to a form usable by digital logic. We propose a system as in Fig. 2, consisting of a generator to create a voltage $V_{\rm in}$, which can vary rapidly depending on the energy environment of the system, a voltage regulator to set the voltage to a desired level, $V_{\rm dc}$, and a DSP load circuit which performs some computation. The desired voltage is set using delay feedback instead of voltage feedback [6]–[8]. Some measure of the performance of the DSP, $f_{\rm dsp}$, based on its critical path delay is compared to a desired performance $f_{\rm clk}$, and $V_{\rm dc}$ is adjusted until that performance constraint is met. In a conventional fixed supply voltage scheme, the supply is at a level high enough to meet the most demanding performance required from the load circuit under worst case process and temperature conditions. However, the supply voltage is often higher than necessary under nominal operating conditions, and the circuit is then idle for some portion of the cycle. The delay (or performance) feedback scheme, on the other hand, compensates for temperature, process, and computational workload variations. It also allows a simple, all digital implementation of the control loop.

In addition to a generator, the self-powered system requires a backup power source providing voltage $V_{\rm bk}$. This is necessary since at startup the voltage regulator must derive its power

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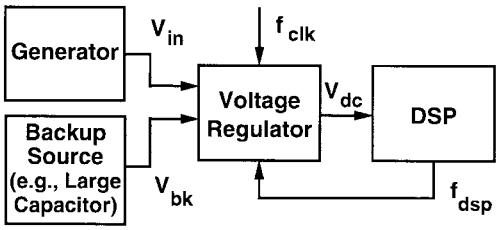

Fig. 2. System block diagram.

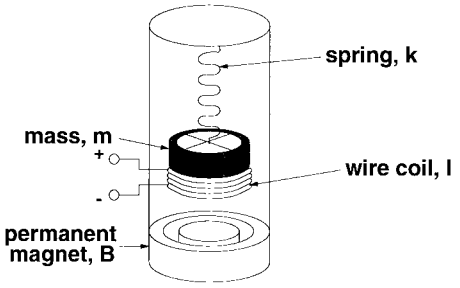

Fig. 3. Generator mechanical schematic.

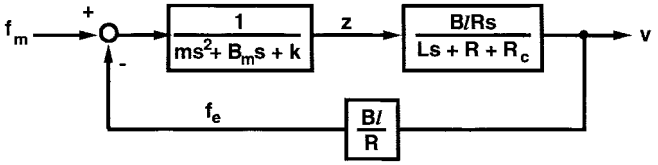

Fig. 4. Block diagram of traditional low-frequency moving-coil transducer model.

from some source and the generator output is too uncontrolled to be used. The source could be a very small battery or a previously charged large capacitor, but it need not provide much energy since it is only used during the startup transient of the system. Another key difference is that the generator output voltage V_{in} varies rapidly with time, in contrast to the slowly drooping battery voltages of conventional systems.

The rest of the paper describes in detail the design, implementation, and test of a self-powered DSP system. Section II describes the particular approach to power generation taken in this study and evaluates its potential for power output. Section III discusses the design of the voltage regulation scheme. Test results for the overall system are shown in Section IV. Finally, Section V concludes and discusses the potential for future work in this area.

II. Power Generation from Mechanical Vibration

Our particular approach to using ambient energy sources for power involves transduction of mechanical vibration to electrical energy. We also performed some side experiments on using incident sound as another power source.

A. Sources of Ambient Energy

Various schemes have been proposed to eliminate the need for batteries in a portable digital system [9]. The most familiar ambient energy source is solar power, but other examples include electromagnetic fields (used in RF powered ID tags [10], inductively powered smart cards [11], or noninvasive pacemaker battery recharging [12]), thermal gradients, fluid flow, energy produced by the human body [13], and the action of gravitational fields [14]. A generator based on transducing mechanical vibrations can be enclosed to protect it from a harsh environment, it functions in a constant temperature field, and a person can activate it by shaking it. However, its moving parts imply less long-term reliability and more complex mechanical design. Applications include sensors mounted on vibrating machinery or worn on the body. Ambient acoustic energy can also be used, but as Section IV-A will show, the high field intensities required make this approach very difficult.

B. Vibrational Power Transducer

An inertial electromechanical generator has been proposed [9]. A mechanical drawing of this generator appears in Fig. 3. The device consists of a mass m connected to a spring k. The other end of the spring is attached to a rigid housing. As the housing is vibrated, the mass moves relative to the housing and energy is stored in the mass-spring system. A wire coil l is attached to the mass and moves through the field of a permanent magnet B as the mass vibrates. The moving coil cuts a varying amount of magnetic flux, which in turn induces a voltage on the coil in accordance with Faraday's Law. This voltage is the electrical output of the generator and is the input to the voltage regulator of Fig. 2.

We have developed a linearized model of the generator by adapting traditional linear models for loudspeakers [15], [16]. Moving coil speakers use a very similar electromechanical transducer to the one proposed for the generator. Fig. 4 shows this model in block diagram form. A mechanical input force feeds into a second-order mechanical system, the spring mass of the generator plus a dashpot with damping coefficient B_m corresponding to the mechanical losses due to friction. The output of the mechanical system is the position of the mass, which feeds into an electrical system corresponding to the wire coil loaded with a resistor R. The electrical system looks like a first-order LR circuit, with the inductance L in series with the load resistance and the parasitic resistance of the coil R_c. The voltage is proportional to the derivative of coil position, so we have a zero at the origin in the system transfer function multiplied by the coil length, the magnetic field, and the load resistance. The currents induced in the coil by the vibration in turn generate an electromechanical force, f_e, that feeds back and damps the mass motion.

The overall transfer function from input force to output voltage is

$$G(s) = \frac{(BlR)s}{(Ls + R + R_c)(ms^2 + B_m s + k) + (Bl)^2 s} \quad (1)$$

but we note that in most cases the electrical pole is much faster than the mechanical dynamics for the vibration cases of interest. The inductance of the coil is small and the load resistance for a low power system is large, consequently, the L/R time constant is short. This corresponds to a fast pole. On the other hand, the mechanical constants are chosen such that the resonant frequency of the generator system is close to the expected input vibration frequencies. These are usually much

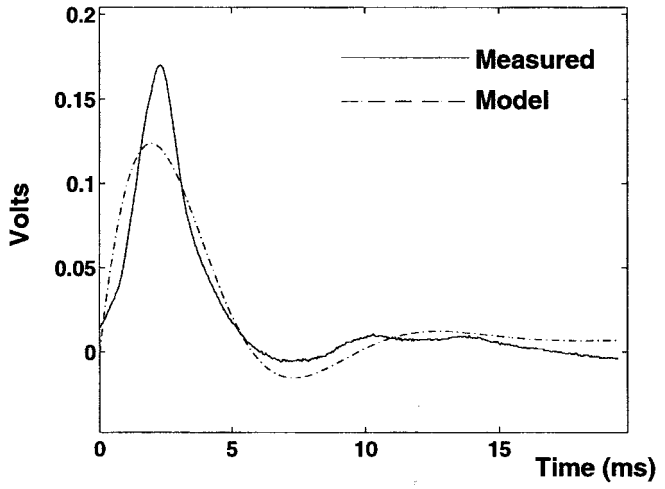

Fig. 5. Measured versus simulated generator response. Mass $m = 0.5$ g and spring constant $k = 174$ N/m. The rms error between the simulated and measured response is 15 mV.

lower than the fast electrical pole. Therefore, it is reasonable to ignore that pole and to treat the linearized system as a damped second-order system. The mechanical and electrical damping coefficients are then lumped together.

A prototype generator following the design of Fig. 3 was built using discrete components. The generator was tested by giving the mass an initial displacement and then releasing it. The coil load resistance was 10 Ω. The resulting voltage output waveform is shown in Fig. 5 and compared to the predicted results from the fitted linearized model of (1). The model captures the basic behavior of the system. In particular, for a mass $m = 0.5$ g and a spring constant $k = 174$ N/M, the resulting natural frequency $f_0 = 94$ Hz, which matches the frequency of the measured output well. Note that this is much less than the electrical pole which was found to be at 1.2 kHz, validating the second-order assumption.

There are several things to note in Fig. 5. First, the peak output voltage of the generator is only 180 mV, which is too small to be rectified by a diode. A transformer is thus necessary to create a large enough voltage from the generator output to be converted by the regulator. Although it is possible to use a diode with a lower turn-on voltage, leakage currents become a problem. Synchronous rectification is also possible but requires sensing of the generator output and rapid switching of the rectifying transistors since the generator voltage varies quickly. A transformer is the simplest electrical solution to this problem.

There are also significant differences in the linear model and the measured output. The rms error between simulated and measured responses is 15 mV. The errors are due to unmodeled nonlinearities in the spring and dashpot, magnetic field variation vertically and in the air gap, and higher order vibrational modes of the system including twisting and flexing of the mass. However, this simple model provides a reasonable baseline for estimating power generation capability and system design.

To increase the peak output voltage, eliminating the need for a transformer, one can vary both the electrical and mechanical parameters. By increasing the number of turns in the coil or by increasing the permanent magnet field, the flux linked by the coil and therefore the voltage can be increased. Increasing the spring constant or reducing the mass will increase the natural frequency of the mechanical system. Since the voltage is proportional to coil velocity, it is also proportional to this natural frequency in excitation situations where the natural modes of the generator dominate, for example, in impulsive shock vibrations. The output voltage will also increase. However, the voltage only scales with the square root of the mechanical parameters whereas it scales linearly with the electrical ones, so it is more advantageous to modify the electrical variables when possible. Also, the mechanical resonant frequency determines how well the ambient vibration couples into the generator as will be discussed below.

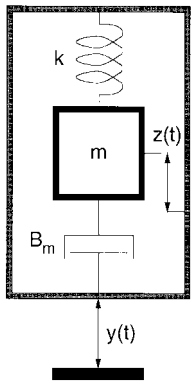

Fig. 6. Simplified generator mechanical dynamics.

C. Power from Ambient Vibration

Using this generator design model, we can evaluate the potential of this approach for batteryless operation of portable electronics. In [17], we presented a frequency domain approach for estimating the amount of power that might be generated from ambient mechanical vibration. An alternative approach is to use a stochastic vibration model to produce a time domain estimate.

Fig. 6 shows a simplified model of the generator. The housing vibration displacement $y(t)$ couples into a relative mass displacement $z(t)$. The electrical and mechanical damping are lumped into one dashpot element. The output power is therefore

$$P_o(t) = B_m \dot{z}^2 \tag{2}$$

where B_m is the lumped dashpot coefficient and $\dot{z}$ is the mass velocity relative to the housing. Suppose a sinusoidal excitation $y(t) = Y_0 \cos(\omega t)$ drives the system. From the well-known theory of linear resonant systems, the output dc power in sinusoidal steady state is

$$P_{\text{out}} = \frac{m\omega_0\omega^2\zeta Y_0^2}{\left\{\left[1-\left(\frac{\omega}{\omega_0}\right)^2\right]^2 + \left(2\zeta\frac{\omega}{\omega_0}\right)^2\right\}} \tag{3}$$

where ζ is the normalized damping coefficient, m is the mass, and ω_0 is the natural frequency of the resonator. Fig. 7 shows frequency domain plots for the average power output for three different values of ζ. Clearly, as ζ increases (the system becomes more damped), the average power has a

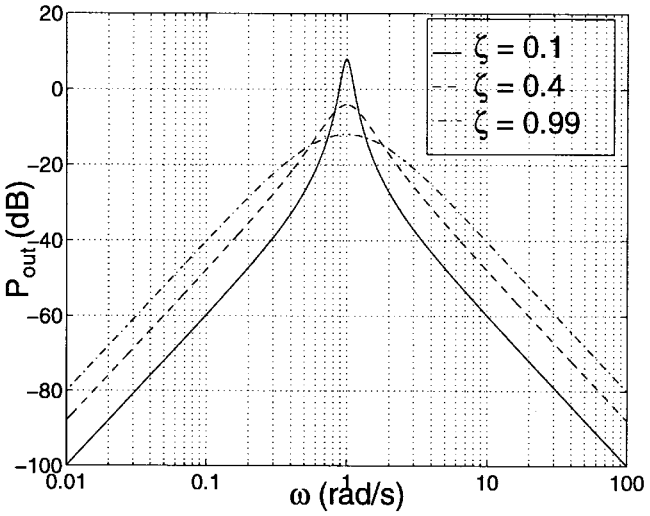

Fig. 7. Frequency domain plot of dc power $P_{\rm out}$ for three different damping coefficients.

broadband characteristic. However, its peak value decreases. This indicates how one can adjust the mechanical parameters m, k, and B_m to optimize the generator output for particular vibration inputs. First, adjust the natural frequency such that it is as close to the input vibration frequencies as is practical. Second, depending on whether the input vibrations are narrow or wideband, adjust the damping coefficient to maximize the output power. Changing m and k shifts the resonant frequency while adjusting the electrical parameters can adjust the total damping. Although the filter is peaked at resonance, input vibrations far away can still result in reasonable power outputs if they have enough energy.

The vibration source we tried to estimate was human walking. We modeled this as a stochastic signal with a narrowband power spectral density centered on 2 Hz [13], [18]. The amplitude of the vibration was limited to less than 2 cm in the vertical direction, roughly corresponding to the motion of something carried in one's pocket. This model for $y(t)$ was simulated to generate an output power time series using (2). This is plotted in Fig. 8 for about 2 s. The average output power dissipated in the dashpot was 400 μW, but this is really a best-case estimate of output power. The mechanical damping was ignored in this case and the generator was optimized by tuning the mechanical resonance of the spring-mass system to the 2 Hz vibration center frequency and minimizing the damping within the constraints of the relative mass displacement. A self-powered system using human walking as a vibrational power source must therefore consume less than 400 μW, which is a very reasonable goal considering the current state of the art in low power VLSI design.

III. Voltage Regulator

Since we are interested in generating power from ambient vibration, $V_{\rm in}$ is going to be a time-varying voltage. Moreover, the vibration source may not be reliable or periodic, as in the case of a person walking or machinery that turns on and off at nondeterministic intervals. To maintain correct functionality at a specified performance level, the input voltage must be regulated to a desired value before it can be used to power a load

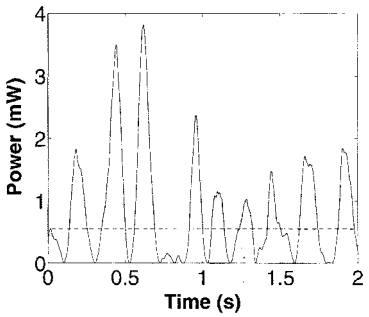

Fig. 8. Stochastic output power simulation: best-case estimate of ambient power generation from vibration due to human walking. Mean output power $\approx$ 400 μW.

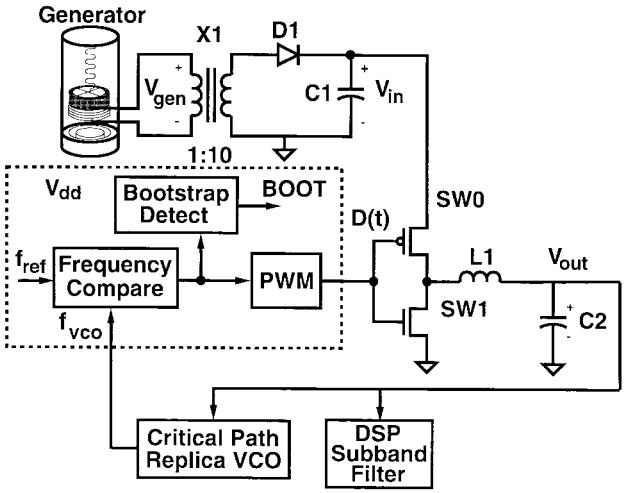

Fig. 9. Detailed block diagram of self-powered DSP system.

circuit. This is done using a very low power dc/dc switching converter. The generator subsystem is designed to produce a high enough voltage that only a down (Buck) converter [19] is required. These converters have successfully been used in low power battery-based applications [20]. However, the controller in the self-powered application must be extremely low power (on the order of a few μW), as opposed to several mW's demonstrated in previous applications.

A. Generator Subsystem

Fig. 9 is a detailed block diagram of the overall self-powered system. The generator and rectifier subsystem is shown at the top. Transformer X1 (with a 1 : 10 turns ratio) converts the output voltage of the generator V_{gen} to a higher voltage than can be rectified by the half-wave rectifier formed by diode $D1$ and capacitor $C1$. Note that with improved magnetic and mechanical materials, the transformer can be eliminated (see Section II-B). Voltage $V_{\rm in}$ is the time-varying input voltage to the regulator.

B. Regulator Architecture

The regulator consists of five main subsystems: a VCO, frequency comparator, pulse-width modulated (PWM) waveform generator, bootstrap detection circuit, and a Buck converter. An external input provides the performance constraint: the rate at which the load circuit must produce results. The load circuit in this case is an 8-bit FIR filter. The DSP rate command is de-

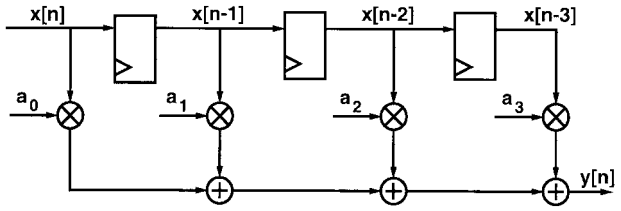

Fig. 10. Subband FIR filter block diagram.

livered in the form of a clock, f_{ref}, the rate at which new input samples are fed to the DSP. Its period therefore corresponds to the total delay between valid output samples of the DSP. To achieve the lowest possible power consumption, the converter downconverts $V_{\rm in}$ to the lowest voltage at which the DSP can run and still produce correct results at the rate set by f_{ref}.

The overall control scheme is similar to a phase-locked loop. The rate f_{ref} is compared to the output of a voltage-controlled oscillator, f_{vco}. The VCO is a ring oscillator consisting of the DSP critical path padded with six inverters. It is powered from the regulated output voltage $V_{\rm out}$. Thus it is a replica of the critical path of the circuit whose power supply is being controlled with some delay margin to account for processing mismatches. The feedback adjusts $V_{\rm out}$ until the period of f_{vco} (i.e., the delay of the equivalent critical path) is just short enough to satisfy the performance demand but not so short as to waste power. The error is represented as a 2-bit digital signal produced by the Frequency Compare block.

The converter is a Buck converter with very small P and N FET's (1200 and 300 μm, respectively; previous designs range from several millimeters [21] to centimeters [20]) controlled by a pulse-width modulated waveform, $D(t)$. A new duty cycle is determined from the frequency error and is generated by the PWM block. Note that since $V_{\rm in}$ can change quite rapidly, especially compared to a battery-powered system, $D(t)$ must be able to change quickly to respond. As $D(t)$ turns the switches SW0 and SW1 on and off, the output of the CMOS inverter is a square wave varying between $V_{\rm in}$ and ground with a changing duty cycle. The modulated $V_{\rm in}$ signal is then passed through an LC lowpass filter ($L = 56$ μH, $C = 10$ μF), external to the chip. The filter is chosen such that its cutoff frequency (6.7 kHz) is much lower than the fundamental of the modulated signal. Thus it only passes the dc component of the signal to produce $V_{\rm out} = D(t)V_{\rm in}$.

Power for the controller, voltage V_{dd} in the figure, initially comes from a backup voltage source. The bootstrap detect block switches the controller to $V_{\rm out}$ when the output voltage is deemed stable.

C. DSP Subband Filter Load Circuit

The DSP load for the self-powered system is a well-known low power subband filter [22]. The block diagram is shown in Fig. 10. It is a four tap FIR filter operating on 8-bit-wide data and implements a lowpass filtering function. Careful choice of the hardwired filter coefficients a_i allows the multiplications to be implemented as simple hardwired shifts and adds, greatly reducing the filter power consumption. The filter implementation consumes 4.75 μW with a 1 V power supply and a 500 kHz clock frequency.

The ring oscillator VCO that provides the DSP performance measurement f_{vco} is a replica of the critical path of this filter. Because of the way the multiplies are implemented, this is a simple 10-bit add plus interconnect required for the shifts.

D. PWM Controller Design

Fig. 11 shows a combined view of the Frequency Compare block and the PWM waveform generator. The PWM block generates $D(t)$ with 6-bit resolution, i.e., 64 different duty cycles. A free running ring oscillator running at the controller voltage V_{dd} sets the frequency of the modulation signal. One fixed edge of the square wave is used to set an R/S flip-flop. A 64 : 1 mux selects an edge delayed by a discrete amount from the reference edge to reset the flip-flop. Using the output of the flip-flop as the modulating waveform $D(t)$, we can control the duty cycle by changing the mux selection bits. This delay-line based duty cycle generation is different from previous digital techniques which use a fast clocked counter [8]. Fig. 12 shows a block diagram of this type of PWM generator. The digital duty cycle value $d[k]$ is digitally compared to a counter output $x[k]$, with the output of the comparator taken as the modulating waveform $D(t)$. The counter is clocked at K times the PWM waveform frequency, where K is the duty cycle resolution. When $x[k] > d[k]$, the comparator output goes low producing the falling edge of $D(t)$. When the counter overflows, $x[k] = 0$ and the comparator goes high, generating the rising edge. This approach is very similar to classic analog PWM, but consumes a lot of power because of the high clock rate for the counter.

The oscillator is free running in this implementation; so as the controller power supply changes (by being switched from the backup voltage $V_{\rm bk}$ to the regulated output $V_{\rm out}$, for example), the frequency of the PWM waveform changes. It can also change due to variations in process and environmental conditions, but these changes are slow compared to the voltage switching. As long as the design maintains this frequency much higher than the LC filter cutoff for all potential supply voltages, this frequency variation is not a major issue for the performance of the switching converter. A variation on this for generating the PWM waveform is to fix the oscillation frequency via a delay-locked loop (DLL). The feedback can fix the frequency of $D(t)$ independent of variations in the controller supply voltage V_{dd}, for example, by proper control of current starved inverters in a ring oscillator. Using the lowest possible frequency for the PWM waveform, just high enough above the cutoff frequency of the LC filter to reduce output voltage ripple to an acceptable value, ensures that the lowest power dissipation is achieved by the PWM waveform. Although the implementation in this system may be less power efficient than a fixed frequency PWM generator using a DLL, it does have reduced complexity by eliminating the DLL control loop. When the overhead of implementing the DLL is considered, it is not clear which approach has the lowest power.

The frequency compare circuitry appears on the left side of Fig. 11. It consists of one 2-bit counter clocked by the performance constraint clock f_{ref}, and one 3-bit counter clocked by the critical path VCO clock f_{vco}. The logic compares the two frequencies by counting the number of edges N of f_{vco} that occur between edges of f_{ref}. Since this

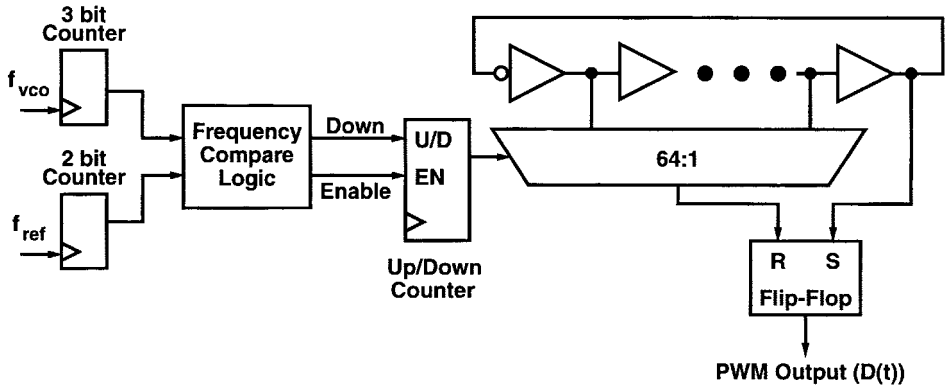

Fig. 11. Low power digital PWM controller architecture.

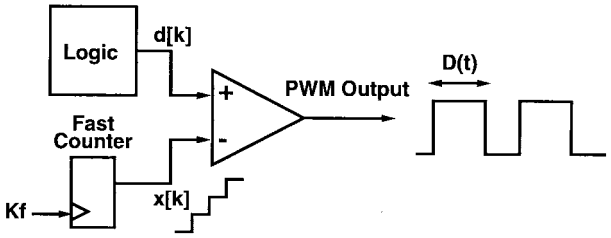

Fig. 12. Fast clocked counter PWM waveform generator. The duty cycle $d[k]$ is digitally compared to the counter output $x[k]$ and the comparator output is used as the PWM waveform.

TABLE I
FREQUENCY COMPARATOR VALUES AND BOUNDS ON f_{vco}

N	Frequency Bounds
0	$0 \leq f_{vco} \leq \frac{f_{ref}}{2}$
1	$0 \leq f_{vco} \leq f_{ref}$
2	$\frac{f_{ref}}{2} \leq f_{vco} \leq \frac{3f_{ref}}{2}$
3	$f_{ref} \leq f_{vco} \leq 2f_{ref}$
≥ 4	$\frac{3f_{ref}}{2} \leq f_{vco}$

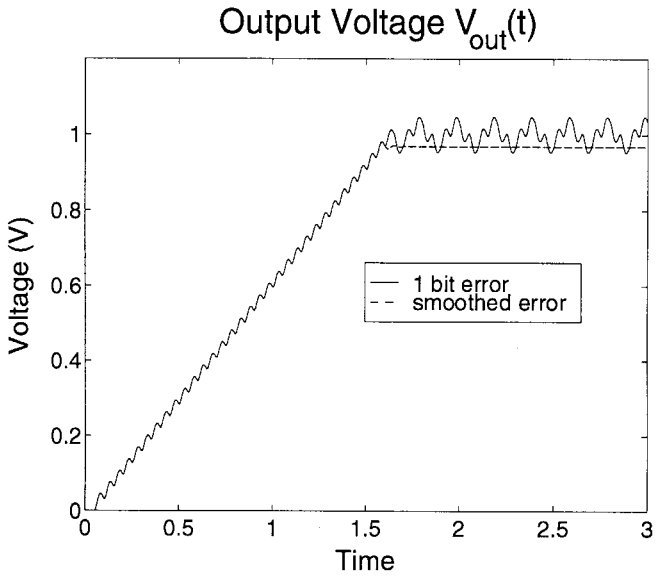

Fig. 13. Limit cycle behavior of low resolution digital control loop. The smoothed error response eliminates the limit cycle, at the cost of steady-state error. The digital duty cycle has 6-bit resolution, for a maximum value of 63.

detector provides no information on the relative phase of the two signals, for each value of N, there is a range of possible frequencies f_{vco} relative to f_{ref}. Table I shows these ranges. For $N \geq 3$, the system meets the specification guaranteeing $f_{vco} \geq f_{ref}$. However, a frequency error of $N \geq 4$ implies that the VCO is running too fast. The controller asserts Down in this case to reduce the duty cycle. For $N \leq 2$, Down is deasserted and the duty cycle increases. Down is used to increment or decrement an up/down counter. This counter effectively integrates the error and its output is used to control the PWM mux. Another signal, Enable, is deasserted if $f_{vco} \approx f_{ref}$, i.e., if $N = 3$. The controller disables the counter and the duty cycle remains unchanged. This technique holds the duty cycle steady if the DSP is just meeting the performance constraint. This smoothes steady-state limit cycles caused by constantly switching the duty cycle value [23].

Fig. 13 shows a simulation of a limit cycle caused by low resolution digital feedback for a voltage referenced loop. The initial system is at rest, with V_{in} of 2 V and a desired V_{out} of 1 V (corresponding to a 50% duty cycle). The 6-bit duty cycle $d[k]$ (for a maximum value of $63/64 \approx 98\%$) is incremented by one as long as the output voltage is less than the reference. It is decremented when the output is higher. When the output gets close, however, the 1-bit resolution of the error causes the duty cycle value to toggle around the desired value. This in turn causes a systematic ripple in V_{out}. The same ripple is seen in the inductor current i_l and the voltage error $e(t)$. Although the error does not increase in amplitude (the system is stable in the sense of Lyapunov), this controller induced ripple is undesirable if its amplitude is too high. Note that there is additional ripple due to the attenuated feedthrough of the higher harmonics of the PWM waveform. The limit cycle can be smoothed by holding the duty cycle constant when the output voltage becomes close enough to the reference. Unfortunately, this can also result in steady-state error if the error threshold of changing the duty cycle is large.

The size of the counters is determined by how accurately the above performance conditions are to be met by the regulator. Increasing the counter sizes allows more careful control of the DSP speed. Since the DSP is intended to run near the edge of subthreshold operation (around 1 V V_{dd} in the case of our process), small voltage changes result in very large frequency variations in f_{vco} but small changes in the total DSP power. Low resolution error measurement is then acceptable

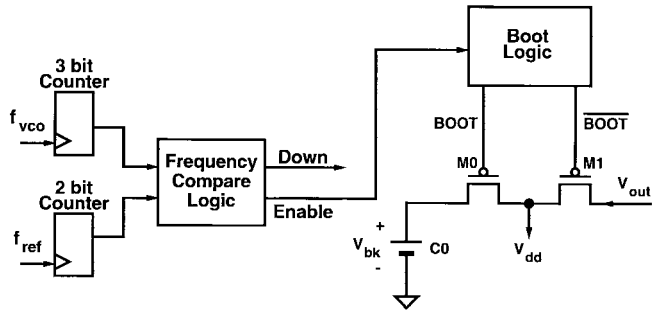

Fig. 14. Bootstrap circuit schematic.

and reduces power consumption in the controller. Metastability in the f_{vco} counter value is handled by latching its output into another register.

To further improve the stability of the loop, the frequency error is subsampled at a rate set by a programmable counter. If the error is sampled too quickly at the low resolution given by the short counters, the controller tends to switch the duty cycle faster than the LC filter can adjust, resulting in widely varying duty cycles and output voltages. This condition effectively destabilizes the loop. By initializing the error sampling counter with different values, the dynamics of the controller can be adjusted to ensure stable loop operation for a given LC filter.

E. Startup Issues

At startup, the controller supply V_{dd} receives its power from the backup source $V_{\rm bk}$—either a battery or a capacitor. The bootstrapping circuit shown in Fig. 14 determines when V_{dd} can be switched to the regulated output voltage $V_{\rm out}$. This is done using the same logic that controls the PWM generator from the frequency error. Enable is deasserted when the reference performance and the DSP load performance are very close, ensuring that the output voltage is held steady. This in turn implies that $V_{\rm out}$ is stable enough to use as the controller power supply. The enable signal is fed into logic that controls a PMOS mux and switches V_{dd} from $V_{\rm bk}$ to $V_{\rm out}$ using the Boot signal and its inverse. If $V_{\rm out}$ drifts too far from the desired value, the controller will switch itself back to the backup supply, as the Enable signal will be asserted when the frequency error becomes large enough.

IV. Self-Powered DSP System Test Results

To demonstrate the feasibility of a self-powered system, a generator, rectifier, and an integrated circuit containing a switching dc/dc converter and an FIR filter were constructed and assembled into a self-powered system. The full self-powered system was tested using both the moving-coil generator discussed above and an acoustic generator to test steady-state operation of the system. This section presents the test results.

A. Power Generation Test

The moving coil generator prototype was tested using the same initial displacement conditions as in Fig. 5. After the voltage was transformed up, the regulator converted the slowly decaying voltage on the rectifier capacitor to a specified level. The total number of operations performed by the load DSP were counted to give a measurement of the number of operations that can be performed using one excitation of the moving coil generator. The results are summarized in Table II.

TABLE II
Test Chip Specifications

Area	2609 μm x 2609 μm
Transistor Count	5 K
Process	0.8 μm CMOS
NMOS Threshold Voltage	$V_{tN} = 0.70$ V
PMOS Threshold Voltage	$V_{tP} = -0.87$ V
Controller Power	5.71 μW ($f_{ref} = 500$kHz, $V_{dd} = 1$V)
Subband Filter Power	4.75 μW ($f_{ref} = 500$kHz, $V_{out} = 1$V)
Switch Drive Power	7.50 μW ($V_{in} = 1.07$V)
1 Generator Excitation	23 ms of valid DSP operation
	11,700 cycles
	2,340 operations

To determine if it is possible to use an acoustically driven generator, a miniature moving coil loudspeaker [24] was used in reverse as a microphone. It was driven by an identical speaker placed very nearby and driven by a function generator. Although sufficient power was generated at around 1 V to run the DSP system, the very high calculated incident field intensity [25] of 114 dB shows that using acoustic energy is limited to very high noise environments (e.g., loud machinery, airports, etc.).

B. Control Loop Performance

The output response to a step change in $V_{\rm in}$ is shown in Fig. 15. The magnitude of the step is 600 mV, going from 0.9 to 1.5 V. After some initial ringing, the output settles except for small low-frequency ripples at the far right of the trace. A limit cycle in the controller due to the low resolution error feedback causes the PWM to oscillate around the correct value. Smoothing has helped reduce the size of the cycle, but has not eliminated it entirely. The size of this limit cycle can be decreased further by changing the error sampling rate as discussed in the previous section.

Fig. 16 shows the correct operation of the bootstrapping circuit at system startup.

C. VLSI Implementation

The FIR filter, power FET's, and PWM control circuitry are all integrated onto a single test chip. The circuits followed established low voltage design principles. All logic is implemented using a static CMOS style, with small P devices, since the switching times can be long because of the long system clock period (2 μs). To reduce clock power, the latches are TSPC designs [26]. Dense layout minimizes interconnect capacitance by reducing routing lengths. HSpice simulations using Level 28 models were used to verify circuit operation at near-subthreshold supply voltages.

The test chip parameters are summarized in Table II. For f_{ref} at 500 kHz, the controller consumes 5.71 μW and the FIR filter and load ring oscillator 4.75 μW at 1 V power supplies.

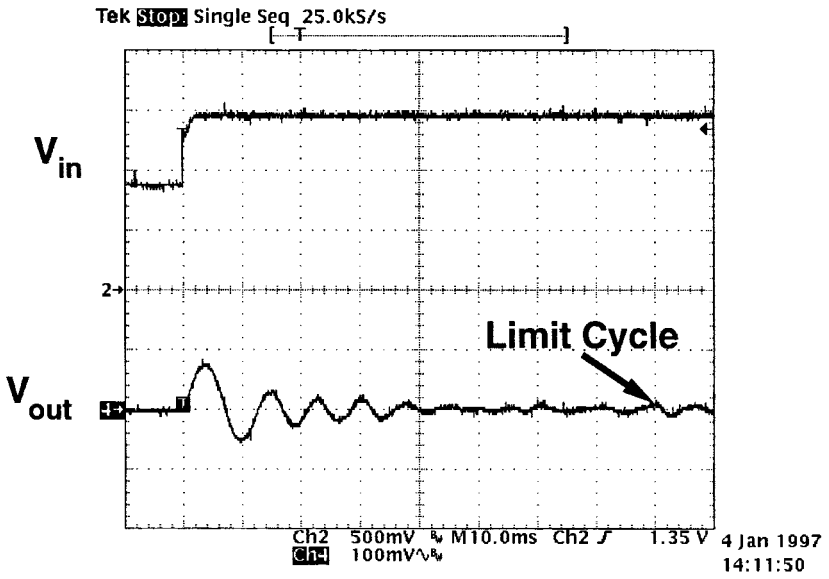

Fig. 15. Step response. Note steady-state limit cycle due to low resolution digital control.

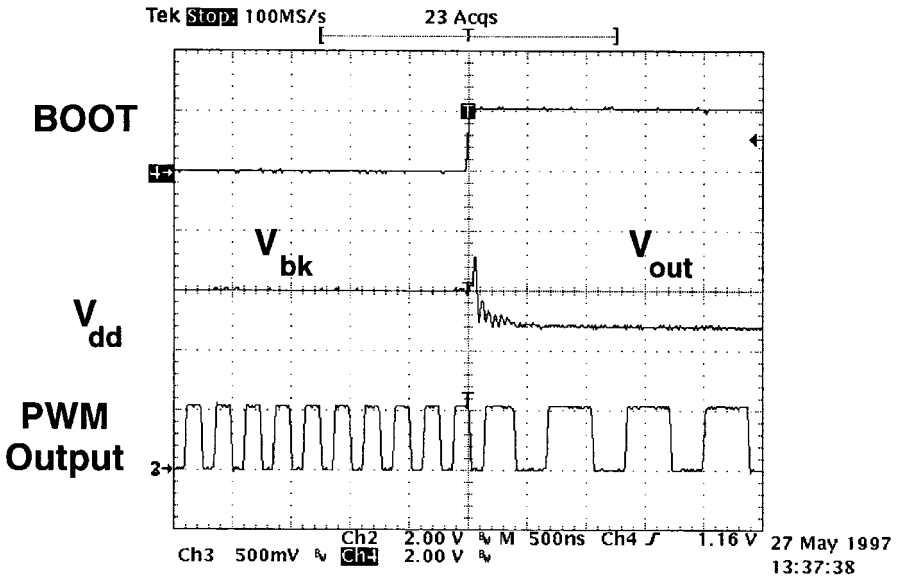

Fig. 16. Bootstrapping.

This does not include switching the PWM output FET's or the chip pads, which consumes a power of 7.5 μW.

A single generator excitation produced 23 ms of valid DSP operation at a 500 kHz clock frequency, corresponding to 11 700 cycles. The clock frequency is consistent with medium throughput sensor applications. A valid output sample appears at each cycle. Since the DSP impulse response contains 4 samples, the generator excitation produces power for 2340 five-cycle impulse response computations. The total energy used by the load was 114 nJ. Looking at the table, it appears that the self-powered system is inefficient, but this is purely a result of having such extremely low power dissipation in the load DSP. The controller power is a fixed cost, and the only part of the switch power that scales with increasing delivered power is the i^2R resistive losses in the switch FET's. HSpice simulations indicate that these losses are small. If the delivered power is increased to 100 μW, the system efficiency becomes greater than 80%. However, the load will run for less time off a single generator excitation. The time is constrained by the slowly dropping voltage on the rectifier storage capacitor; at some point, it becomes too low for the DSP to meet the f_{ref} performance constraint. The time of valid DSP operation thus decreases linearly with the delivered current.

A die photo is shown in Fig. 17. The chip integrates the load DSP, the critical path VCO, the regulator circuit, and the power switches. The controller is fairly simple, requiring only 2247 transistors out of the 5k total number.

V. Conclusion

A prototype DSP system powered by its own generator and low power voltage regulator has been constructed. Since

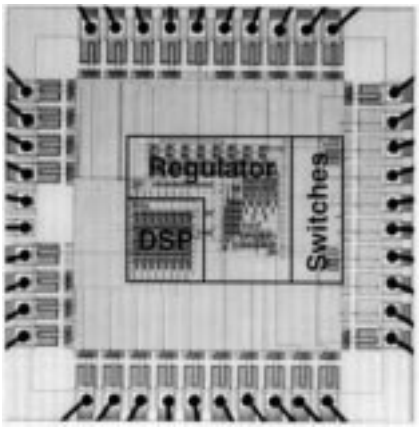

Fig. 17. Die photo.

generated power on the order of 400 μW is feasible, it has been shown that a portable digital system can be powered entirely from ambient vibrations in its environment, thus eliminating reliance on a battery.

Future potential for this work includes more careful modeling of the moving coil generator, so that more efficient generators can be designed and the need for a transformer can be eliminated. A MEMS-based implementation of the generator technology would allow the entire system to be integrated on one die, greatly reducing its cost and size.

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