Adaptive Body Bias for Reducing Impacts of Die-to-Die and Within-Die Parameter Variations on Microprocessor Frequency and Leakage

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***Abstract*—Bidirectional adaptive body bias (ABB) is used to compensate for die-to-die parameter variations by applying an optimum pMOS and nMOS body bias voltage to each die which maximizes the die frequency subject to a power constraint. Measurements on a 150-nm CMOS testchip which incorporates on-chip ABB, show that ABB reduces variation in die frequency by a factor of seven, while improving the die acceptance rate. An enhancement of this technique, that compensates for within-die parameter variations as well, increases the number of dies accepted in the highest frequency bin. ABB is therefore shown to provide bin split improvement in the presence of increasing process parameter variations.**

***Index Terms*—Body bias, CMOS digital integrated circuits, forward bias, low-power circuits, microprocessors, parameter variations, substrate bias, within-die variation.**

I. Introduction

POWER density has become a significant concern in microprocessor design due to the large numbers of transistors integrated in a single die and the increasing clock frequencies. The power density limit of a processor, which is dictated by the thermal design of the system, impacts system cost and maximum operating frequency. Power constraints are even more stringent in mobile processor designs in which long battery life is desirable. At the same time, processors must achieve high frequencies under this power constraint. The goal of a processor design, therefore, is to achieve the maximum operating frequency while meeting the power density constraint.

Process parameter variations result in fabricated dies with variations in maximum operating frequency and power consumption [1], [2]. Within-die variations cause differences in transistor characteristics across a single die. In addition, distribution of device parameters change from die to die within a wafer and across multiple wafers and lots. Together, these variations result in a distribution of die frequencies and leakages. Normally the distribution is divided into several regions, or “bins” and microprocessors are placed into the highest-possible frequency bin that meets the power specification. Some dies cannot be accepted because of either low operating frequency or excessive power consumption.

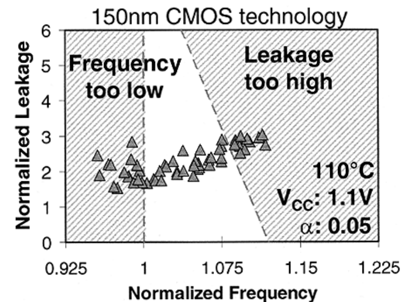

Fig. 1. Measured leakage power and frequency for 62 dies.

Fig. 1 shows the measured frequency and leakage for 62 testchip dies on a single wafer. Due to both die-to-die and within-die parameter variations, there is significant variation in both frequency and in leakage power. In order to be accepted, each die must meet a minimum frequency requirement (represented by the vertical dashed line). At the same time, each acceptable die must meet the maximum power consumption requirement. Assuming a worst-case power density of 20 W/cm^2, the maximum allowed leakage power for each die can be calculated using the die frequency, switched capacitance and a worst-case activity factor α. Any die with leakage power exceeding the maximum allowed at its frequency of operation violates the total power constraint. This die must be either accepted at a lower operating frequency, or discarded if the standby leakage power (I_{SB}) limit is exceeded. A significant number of dies become unacceptable since they fail to meet one of these two constraints.

The leakage and frequency for a single die can be controlled to some extent using body bias, which employs a non-zero body-to-source bias to modulate the threshold voltage of a transistor. Reverse body bias (RBB)[3]–[5] has been employed in recent years as an effective technique for reducing the leakage power of a design in standby mode by raising the voltage of the pMOS *N*-wells with respect to the supply voltage, or by lowering the voltage of the substrate relative to ground. Similarly, forward body bias (FBB) [6]–[8] has been used in active mode to increase the operating frequency of a design, although this increases the leakage power as well. In addition, FBB has the desirable result of improving the short-channel effects of a transistor, thus reducing sensitivity to critical-dimension variation [9].

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By controlling the transistor threshold voltages (V_T) through process adjustment or body bias, the distribution can be moved to the left (by raising the V_T) or to the right (by lowering the V_T). Ideally, the V_T should be lowered for dies that are too slow and raised for dies that are too leaky, maximizing the number of dies in the middle of the distribution that meet both frequency and leakage constraints. This can be accomplished through the use of bidirectional adaptive body bias (ABB) [9]–[12]. This bidirectional ABB technique is described in Section II and a specific testchip implementation is detailed. Measurement results from this ABB test chip are used throughout this paper to demonstrate the effectiveness of ABB. Section III describes a method for correcting die-to-die variations using ABB and measurements show the resulting effect on die acceptance percentage, frequency and leakage power. The effects of within-die parameter variation are explored in Section IV and an enhancement of the ABB technique is presented which compensates for these variations as well. Finally, Section V concludes the paper by summarizing the improvements in die acceptance rate and processor frequency made possible by ABB.

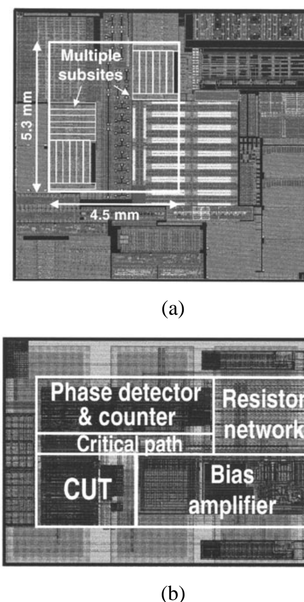

Fig. 2. (a) Die micrograph, noting locations of testchip subsites. (b) Micrograph of a single testchip subsite.

II. ABB Implementation

Bidirectional ABB allows each die on a wafer to have the optimum threshold voltage which maximizes the die frequency subject to the power constraint. The threshold voltage of each die is controlled not only by process but also by the application of the appropriate amount of FBB or RBB. Dies which are too slow receive FBB, increasing the die frequency as well as the die leakage. Dies that violate the leakage constraint receive RBB, reducing the leakage as well as the frequency. In this way, the combined effect of parameter variations is compensated by changing the V_T of the devices. In leakage-sensitive circuit topologies, such as dynamic circuits, it is recommended that the amount of forward bias applied be limited by noise constraints, if the die is too slow but the transistors in those circuits already have a low threshold voltage.

The pMOS and nMOS body bias voltages which result in this optimum threshold voltage may be applied by an external source or by an on-chip body bias generator. Similarly, the control circuitry that determines the optimum body bias voltage may be implemented off-chip or integrated in the die. We have implemented a testchip that incorporates the body bias generator and control circuitry for pMOS devices on die and allows off-chip control and biasing for the nMOS devices. This testchip has been fabricated in 150-nm CMOS technology and demonstrates the effectiveness of bidirectional ABB.

A. Testchip Components

Each testchip die [Fig. 2(a)] contains 21 "subsites" distributed over a 4.5 $\times$5.3 mm^2 area in two orthogonal orientations. Each of these subsites [Fig. 2(b)] represents a circuit block of a microprocessor design and contains a complete ABB generator and control circuit in addition to critical path circuit blocks. The organization of a testchip subsite is shown in Fig. 3. The circuit block, or CUT, contains key circuit elements of a microprocessor critical path, meant to model the effect of body bias on the frequency and leakage of a real microprocessor design.

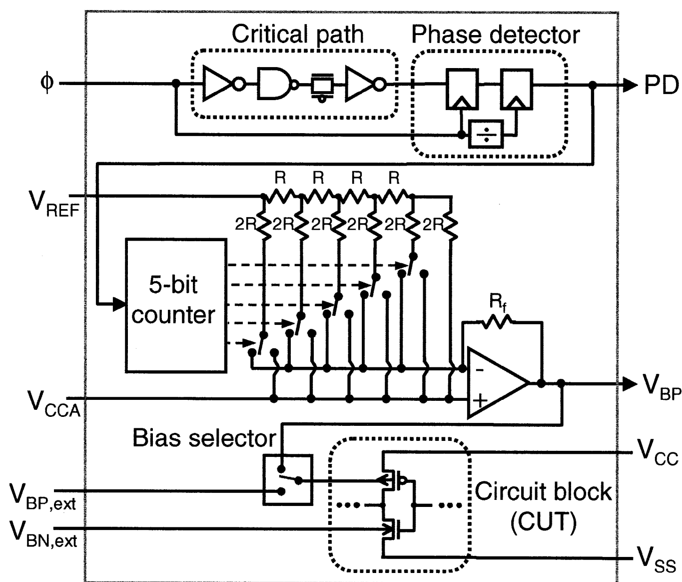

Fig. 3. Block diagram of ABB testchip.

This circuit block can be configured in a ring-oscillator structure for frequency measurements, or disabled to allow leakage power measurements. One critical path from this circuit block is replicated and a target clock frequency ϕ is applied externally. This represents the desired frequency of operation for the circuit block. The output of the critical path is sampled by a phase detector structure consisting of two flip-flops which compare the critical path delay with the target clock period. The output of the first phase detector flip-flop is sampled by a second flip-flop clocked with a divided clock signal. This allows sufficient time for the body bias generator to stabilize and the critical path frequency to adapt to the new body bias before the phase detector is updated again. The output from this second flip-flop, denoted "PD," is used to clock a 5-b digital counter whose value represents the desired body bias to apply. Finally, it is necessary to

Bias Mode	Condition	Range
NBB → FBB	$V_{CCA} = V_{CC}$ $V_{REF} > V_{CCA}$	FBB: 0 → V_{REF}-V_{CCA}
NBB → RBB	$V_{CCA} = V_{CC}$ $V_{REF} < V_{CCA}$	RBB: 0 → V_{CCA}-V_{REF}
FBB → RBB	$V_{CCA} < V_{CC}$ $V_{REF} < V_{CCA}$	FBB: V_{CC}-V_{CCA} → RBB: $2V_{CCA}$-V_{REF}-V_{CC}

Fig. 4. Bias modes provided by on-chip body bias generator.

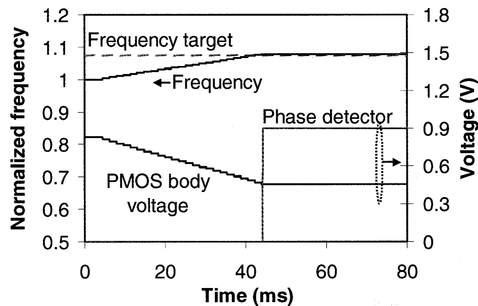

Fig. 5. Adaptive bias operation.

convert this 5-b digital code to an analog body voltage which is applied to the pMOS transistors in both the CUT and in the critical path. This is accomplished through the use of a D/A converter consisting of an R-2R resistor network and an op-amp driver. The output voltage of this body bias generator, which biases the pMOS transistors in the CUT and in the critical path, is a function of the 5-b counter value as well as the supply voltages $V_{\rm REF}$ and $V_{\rm CCA}$. Different ranges of unidirectional—FBB or reverse —or bidirectional body bias values (Fig. 4) can be selected by using appropriate values of $V_{\rm REF}$ and $V_{\rm CCA}$ and by setting a counter control bit. For the desired body-bias range of 500-mV RBB to 500-mV FBB, (a range of 1 V in 32 steps) this bias generator can achieve 32-mV bias resolution. ABB can also be accomplished by using the phase detector output to continually adjust off-chip bias generators through software control, instead of using the on-chip circuitry, until the frequency target is met.

B. Testchip Operation

For a specific, externally applied nMOS body bias, this on-chip circuitry automatically generates the pMOS body bias that minimizes leakage power of the CUT while meeting a target clock frequency. An example of measured testchip operation is shown in Fig. 5. Initially, the operating frequency of the circuit block is lower than the desired target frequency. The body voltage therefore reduces, forward-biasing the pMOS transistors and increasing the frequency. This continues until the circuit frequency matches the desired frequency target, at which point the phase detector output switches to a one, disabling the counter. This adaptation process is done at high temperature since this represents the worst-case frequency of the part as well as the largest leakage power expected. Once the optimum bias voltages are determined, they may be permanently programmed into the chip in the case of an on-chip bias generator, or programmed into the external voltage regulators supplying the off-chip bias voltage.

III. Die-to-Die ABB

Using only a single pMOS/nMOS body bias combination per die, ABB can be used to compensate for die-to-die variations. The goal of the ABB procedure is to find the optimum pMOS/nMOS bias combination that maximizes the die frequency while meeting the leakage constraint. Because each subsite represents a critical path of a microprocessor design, the die clock frequency is the minimum of the CUT frequencies and active leakage power is the sum of the CUT leakages. We have evaluated several ABB techniques through measurements on 21 CUTs per die at 1.1 V $V_{\rm CC}$ and 110 °C, for 62 dies on a wafer.

A. Simple ABB (S-ABB)

In the simplest ABB scheme, the optimum bias voltages are determined through measurements on a single circuit block on the die. Consider, for example, a microprocessor consisting of many large circuit blocks, each of which is equally critical. One of these circuit blocks contains a replica critical path and a phase detector which communicates with a central body bias generator. Based on the frequency of this critical path, the central bias generator determines the body bias which must be applied to meet a target frequency and this body bias is applied to all circuit blocks on the die. Because the optimum body bias is determined through measurement on a single circuit block, this method therefore ignores any within-die variation that results in differences in frequency and leakage among circuit blocks fabricated on the same die.

The central bias generator, along with the required body bias buffers and additional bias routing, incurs $\sim 2\%$ total die area overhead [6]. Because the current in the transistor body is at least two orders of magnitude smaller than the supply current, the body bias grid is significantly less dense than the supply grid. The body bias buffers, which are distributed throughout the die, are designed so that the body bias voltage tracks variations in the local supply voltage of each circuit block. In addition, these buffers ensure that any noise coupled to the body bias grid does not exceed the expected noise for a design without body bias. No noise-related effects have been observed through measurements of body-biased circuits when compared to traditional implementations without body bias [6].

The optimum bias combination is determined by applying a target clock frequency to the die. This represents the highest-possible operating frequency for the die under the given power constraint, achievable only when leakage power is zero. This maximum clock frequency is shown on Fig. 1 as the intercept of the slanted leakage line with the frequency axis. For that target frequency, an nMOS bias is applied from an off-chip source and the on-chip control circuitry is enabled to automatically adapt the pMOS body bias to meet the frequency target. The leakage power for this combination is measured and the process repeated for all nMOS bias levels. The combination which results in lowest leakage is chosen as the best choice

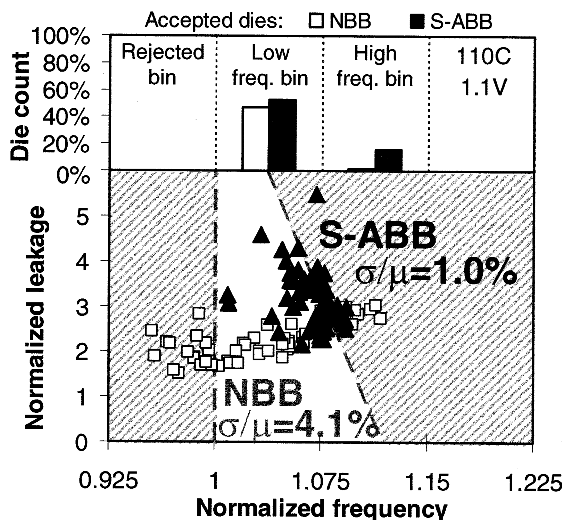

Fig. 6. Leakage versus frequency distribution for NBB and S-ABB.

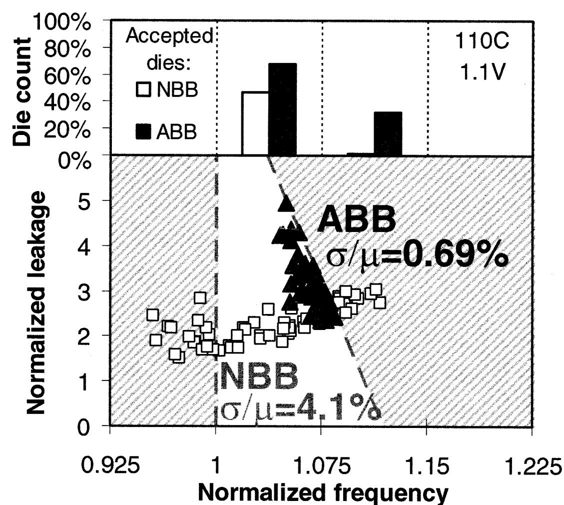

Fig. 7. Leakage versus frequency distribution for NBB and ABB.

for the target frequency and the leakage is compared to the maximum allowed leakage for that circuit block. If the leakage is higher than the constraint, the frequency target must be lowered and the process repeated. Otherwise, the optimum bias combination has been found.

The effect of S-ABB is shown in Fig. 6. The leakage versus frequency distributions for NBB and S-ABB are shown on the bottom plot, while the histogram shows the number of acceptable dies in each frequency bin for the two techniques. Here the frequency range is divided into two acceptable bins and the sum of the two bins gives the total number of accepted dies. When no body bias (NBB) is used, only 50% of the dies are acceptable, mainly in the lowest frequency bin. ABB applied to the same 62 dies reduces the frequency variation σ/μ from 4.1% to 1.0%, resulting in a larger number of accepted dies and more dies in the highest frequency bin. However, there are still a significant number of dies which fail to meet the leakage constraint. These arise from the fact that a single circuit block is used to determine the body bias for the entire die, while within-die variations cause differences in circuit block frequency and leakage.

B. Die-to-Die ABB

An improved ABB technique takes these within-die variations into account when determining the best pMOS/nMOS bias combination per die. The technique is similar to S-ABB except that each circuit block requires its own phase detector structure and the central bias generator takes into account each phase detector output when determining the appropriate body bias voltage. This can be accomplished by combining the individual phase detector signals with an "OR" structure so that the bias generator counter is updated if any circuit block does not meet the target frequency. Area overhead is slightly higher than for S-ABB due to the additional phase detectors required, but still only 2%–3% of the total die area. This technique therefore works in the presence of within-die variations, as demonstrated in Fig. 7. When compared to NBB, ABB reduces the frequency variation σ/μ to 0.69%, resulting in 100% acceptable dies. Furthermore, 32% of the dies now fall

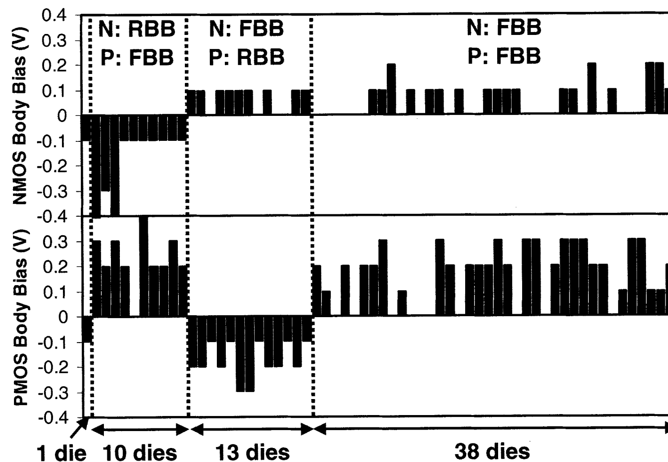

Fig. 8. Histogram of applied bias voltages for ABB.

in the highest frequency bin. Therefore die-to-die ABB results in an increase in the number of acceptable dies, as well as a net frequency increase. It is evident, however, that in order to be most effective, within-die variations must be considered.

The distribution of body bias voltages resulting from ABB is shown in Fig. 8. The 62 dies are grouped into four categories based on the pMOS and nMOS bias required. A majority of the dies (38) receive forward or zero bias for both pMOS and nMOS transistors, while a smaller number require a combination of forward and reverse bias. Only a single die uses reverse bias for both pMOS and nMOS transistors. In addition, a modest bias range is required −300 mV of forward or reverse bias is sufficient for most dies.

IV. Within-Die Variation Compensation

By comparing the results of S-ABB and ABB, it is evident that within-die variations influence the effectiveness of the ABB technique. In this section, we examine the impact of within-die variations as technology scales and describe a method of compensating these variations as well.

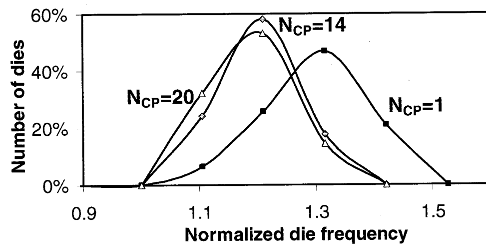

Fig. 9. Die frequency distribution versus number of critical paths ($N_{\rm CP}$) per die.

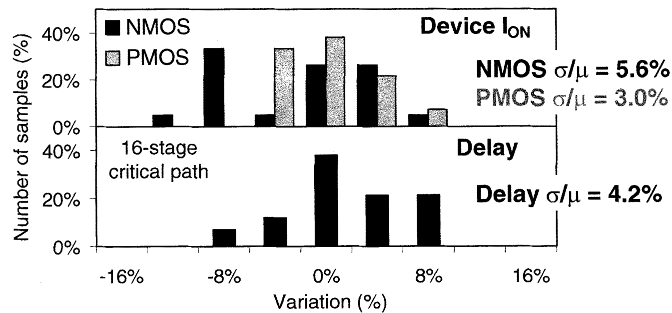

Fig. 10. Device $I_{\rm ON}$ variation versus critical path delay variation.

A. Effects of Within-Die Variation

The relative impacts of die-to-die and within-die parameter variations depends on the number of critical paths ($N_{\rm CP}$) per die. In [2] it is shown through statistical simulations that as the number of critical paths per die increases, the within-die delay variation causes the mean frequency μ to reduce while the variation σ in critical path delays reduces as well. This is confirmed through testchip measurements as shown in Fig. 9. As the number of critical paths per die increases from 1 to 14, the mean frequency reduces by $\sim$ 8% and σ reduces as well. As $N_{\rm CP}$ exceeds 14, however, there is no significant change in the frequency distribution. Because the effect of $N_{\rm CP}$ on die frequency saturates above $N_{\rm CP} = 14$, using measurements of 21 critical paths per testchip die to determine die frequency is sufficiently accurate for obtaining frequency distributions of microprocessors which contain 100's of critical paths.

The impact of within-die variations is also a function of the number of gate stages in the critical paths. Previous measurements [10] on 49-stage ring oscillators showed that σ of the WID frequency distribution is $4\times$ smaller than σ of the device saturation current ($I_{\rm ON}$) distribution. However, measurements on the testchip containing 16-stage critical paths (Fig. 10) show that σ's of WID critical path delay distributions and nMOS/pMOS $I_{\rm ON}$ distributions are comparable. Since typical microprocessor critical paths contain 10–15 stages and this number is reducing by 25% per generation [13], impact of within-die variations on frequency is becoming more pronounced.

B. Within-Die ABB (WID-ABB) Technique

While the improved ABB scheme considers within-die variations in determining the optimum bias combination per die, it is not possible to compensate for these variations using only a single bias combination per die. The WID-ABB technique allows each large circuit block in the design to have its own unique bias combination which controls the frequency and leakage of only that circuit block. Therefore, in this technique, each circuit block requires its own phase detector as in ABB, while the central bias generator must be capable of generating several bias voltages and selecting the appropriate bias for each circuit block on the die. Alternately, the adaptation circuitry from the central bias generator may be distributed as well, although a central bias generator is still required to generate a PVT-invariant reference voltage. In the WID-ABB scheme, each subsite independently adjusts its own body bias to meet the applied frequency target and therefore the total die leakage is minimized for the target frequency. For nMOS implementation, a triple-well process is necessary. While this technique requires a more complex central bias generator, the area of this block is amortized over the entire die and thus the area overhead is similar to ABB.

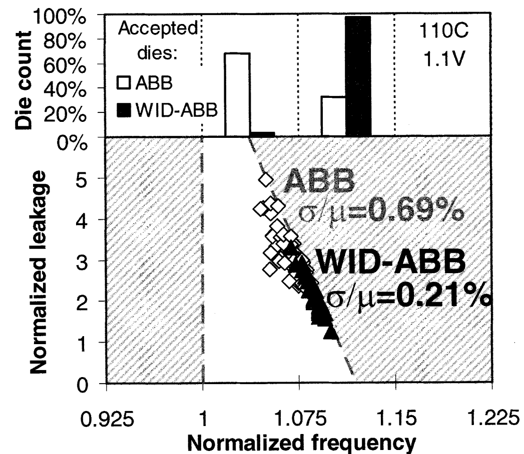

Fig. 11. Leakage versus frequency distribution for die-to-die ABB and WID-ABB.

Fig. 11 shows the effect of WID-ABB when compared to the ABB scheme. The frequency variation has been further reduced by a factor of 3 and again all dies are accepted. In addition, 99% of the dies are now accepted in the highest frequency bin, compared to 32% for ABB. By using multiple bias voltages per die, precise control over the die frequency and leakage is possible. The result is an improvement in die acceptance rate and in frequency bin split. A histogram of optimum body bias voltages for circuit blocks on several adjacent dies (Fig. 12) shows that a significant number of blocks receive RBB for both pMOS and nMOS transistors, enabling large leakage savings. In addition, FBB is mainly required for the pMOS devices. This suggests that the skew for this wafer favors fast nMOS and slower pMOS devices, which is corrected using body bias. The bias distribution changes from wafer-to-wafer and from lot-to-lot as the processing conditions change.

The complexity and overhead of the body bias generator and control circuitry depends on the required resolution in body bias voltage. Fig. 13 shows the effect of bias resolution on the effectiveness of the ABB and WID-ABB techniques. It is evident that 300-mV bias resolution is sufficient for die-to-die ABB while 100-mV resolution is required for WID-ABB. The 32-mV resolution provided by the on-chip bias generator is therefore sufficient for either application.

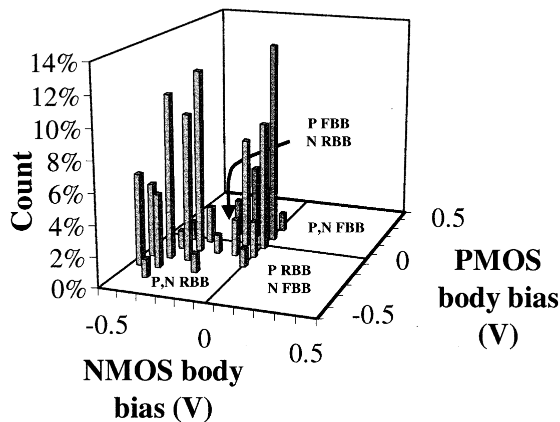

Fig. 12. Histogram of applied body biases for circuit blocks using WID-ABB.

Bias resolution	ABB		WID-ABB	
	dies, F > 1	σ/μ	dies, F > 1.075	σ/μ
500mV	79 %	2.87 %	2 %	1.89 %
300mV	100 %	1.47 %	66 %	0.50 %
100mV	100 %	0.69 %	97 %	0.21 %

Fig. 13. Effect of bias resolution on effectiveness of ABB and WID-ABB.

V. Conclusion

The bidirectional ABB technique has been shown to reduce the effects of process parameter variations on the frequency and leakage of microprocessor dies. Using a single body bias value per die, ABB reduces σ of the die frequency distribution by $7\times$, compared to NBB, allowing all dies to meet the given minimum frequency and maximum power constraints. The number of high-frequency parts can be further increased by the application of WID ABB, reducing σ of the die frequency distribution by an additional $3\times$ and allowing virtually 100% of the dies to be accepted in the highest frequency bin. The ABB technique therefore allows die acceptance rate and bin split improvement in the presence of increasing process parameter variations.

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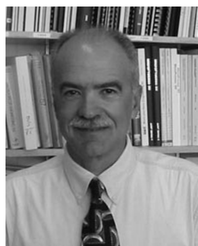

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