A 6.5-GHz Energy-Efficient BFSK Modulator for Wireless Sensor Applications

SeongHwan Cho, *Member, IEEE,* and Anantha P. Chadrakasan, *Fellow, IEEE*

***Abstract*—A 6.5-GHz FSK modulator suitable for low power wireless sensor network is presented. The energy efficient modulator employs closed-loop direct VCO modulation to achieve high data rate, multistage variable loop bandwidth technique for fast startup time and Σ-Δ for reduced power consumption in the synthesizer with fine resolution in frequency channel selection. The modulator, implemented using 0.25-μm CMOS, achieves 20-μs startup time with an effective data rate of 2.5 Mb/s while consuming 22 mW.**

***Index Terms*—Fractional-N, frequency modulation, frequency shift keying, frequency synthesizer, low power, phase-locked loop, sigma-delta modulation, transmitter.**

I. Introduction

EMERGING distributed wireless microsensor networks will enable the reliable and fault tolerant monitoring of the environment. Such microsensors are required to operate for years from a small energy source, while maintaining a reliable communication link with the base station. The constraints of the sensor network are quite different from those of conventional wireless handheld devices. First of all, sensors have small packet size ($\sim$ hundreds of bits) and low average data rate ($\sim$ hundreds of bits/s) due to low event rates. Second, the transmission distance is very short, typically on the order of ten meters or less. Third, the communication link is highly asymmetric (i.e., traffic flow is mostly up-link from the sensors to the base station). Last and most important, sensors are typically required to operate for years from a small energy source and therefore, the energy consumption of the sensor network must be minimized. Due to such unique characteristics of the sensor network, design methodologies for conventional wireless devices would result in inefficient use of energy if they are applied to microsensor network. Hence, various levels of system design hierarchy, from software algorithms and communication protocols to circuit techniques, must be explored to maximize the lifetime of the sensor network [1]–[3]. In this paper, techniques to reduce the energy consumption of the sensor's transmitter will be investigated.

Implementing an energy efficient transmitter is different from designing a low-power transmitter. Since maximizing the battery lifetime is the ultimate goal, energy consumption, rather than power dissipation, must be minimized. The energy consumption of a transmitter when sending a packet size of L bits at R bits/s can be represented by

$$E_{\rm tx} = (P_{\rm tx} + P_{\rm out})\frac{L}{R} + P_{\rm tx}T_{\rm start} \tag{1}$$

where $P_{\rm tx}$ is the power consumption of the transmitter, $P_{\rm out}$ is the power consumption of the output power amplifier and $T_{\rm start}$ is the startup time of the transmitter. In order to reduce the energy consumption, it is important to reduce the transmit time and the startup time as well as lowering the power consumption of the transmitter. Due to sensor's low duty cycle activity, small packet size and short communication distance, the impact of startup time on energy consumption can be significant. This is shown in Fig. 1, where energy consumption per bit is plotted versus startup time. It can be seen that as the startup time is increased, energy consumption is dominated by the startup time rather than the actual data transmission time. Therefore, implementing an energy efficiency transmitter for a microsensor implies designing a high-data-rate, low-power, and fast-startup transmitter. In the following sections, each of these tasks will be examined and accomplished by exploiting architectural and circuit level tradeoffs between the transmitter components.

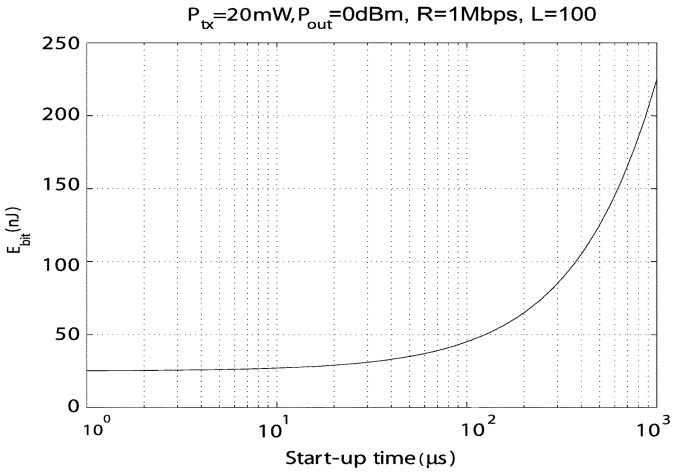

Fig. 1. Effect of startup time on transmitter's energy consumption.

II. High-Data-Rate Low-Power FSK Modulator

A simplified block diagram of the proposed modulator is shown in Fig. 2. The frequency synthesizer is a fourth-order PLL with a third order Σ-Δ for fractional channel selection of the reference frequency. The fractional-N synthesizer allows high reference frequency that is needed to achieve fast startup

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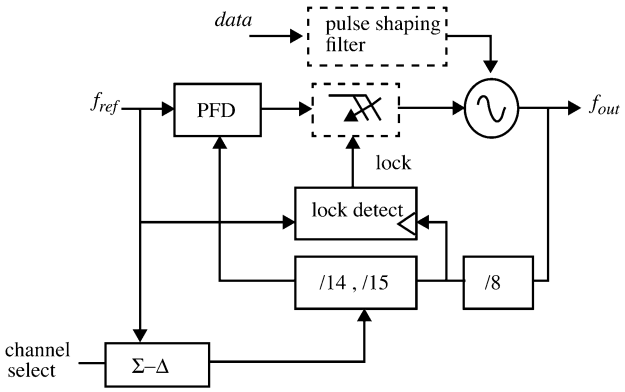

Fig. 2. Proposed BFSK modulator architecture.

time. High-data-rate FSK modulation is achieved by directly modulating the VCO in closed loop. Fast startup time is achieved by employing variable loop bandwidth technique that changes the loop parameters from a large bandwidth to a small bandwidth as the PLL approaches lock.

A. Closed-Loop Direct VCO Modulation

Continuous phase modulation is suitable for sensor communication since low-power implementation is feasible. Several papers have been published on low-power high-data-rate transmitter architectures for continuous phase modulated signals. The indirect modulation method that uses Σ-Δ in fractional-N synthesizer [4] is well suited for such modulation scheme and has spawned other interesting architectures where the data is pre-emphasized [5] and the loop gain mismatches are automatically calibrated [6]. However, as the data rate and carrier frequency get higher, these architectures will consume more power mainly due to the Σ-Δ, high frequency dividers and quantizers. Another architecture that allows compact form of continuous phase modulation is the open-loop direct VCO modulation architecture [7]. Although this method allows data rate that is not limited by the loop bandwidth of the PLL, it suffers from the fact that the output frequency is very susceptible to undesired perturbation and noise, which leads to the use of off-chip components to isolate the VCO, thereby prohibiting the possibility of an integrated chip solution [7], [5].

Closed-loop direct VCO modulation on the other hand is robust to these problems and still has the advantage that the upper bound on data rate is not affected by the PLL loop bandwidth [8]. The drawback however, is that the modulated waveform will be distorted by the negative feedback loop of the PLL. Since the PLL acts as a high pass filter when viewed from the VCO, low frequency components of the modulated data will be corrupted by the PLL. The effect of PLL on modulation can be alleviated by employing Manchester encoding that removes the low frequency component of the data. The resulting performance of the closed-loop direct VCO modulation is plotted in Fig. 3, where bit error rate (BER) is plotted versus signal-to-noise ratio (SNR) for different $\omega_c T$, where ω_c is the loop bandwidth of the PLL and T is the symbol period. It can be seen that the BER improves as $\omega_c T$ gets small. For an $\omega_c T$ of 0.05, less than 2 dB degradation in SNR is seen compared to the ideal case. Since the RF output power for sensors is small (less than 0 dBm), the required increase in the RF output power to overcome this degradation is also small. (i.e., for 0 dBm output power, only 0.6 mW increase in the output power is needed to raise the SNR by 2 dB) Hence, the SNR degradation from closed-loop modulation can be considered acceptable for sensor applications that have short transmit distance.

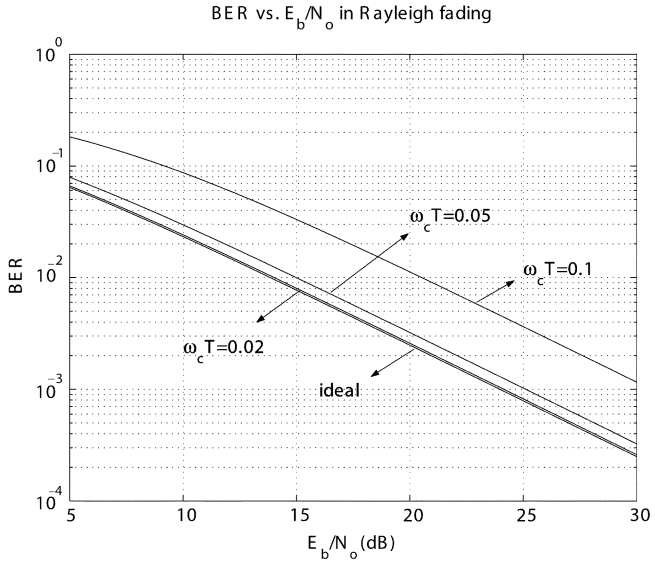

Fig. 3. BER of closed-loop modulation in a Rayleigh fading channel.

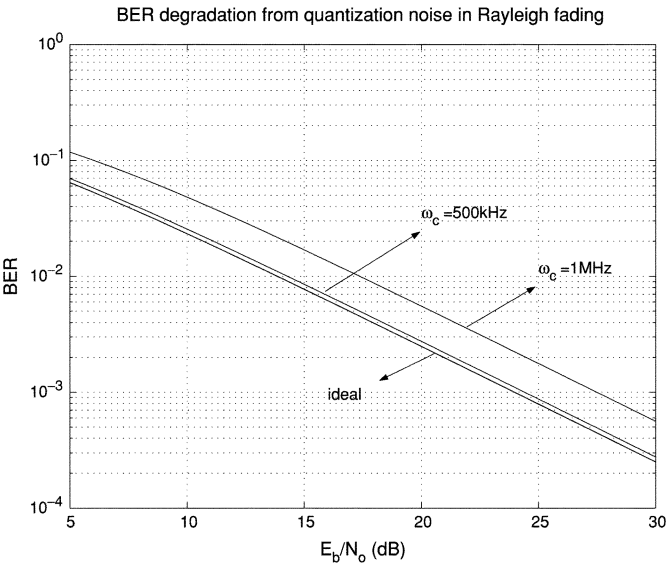

Fig. 4. BER degradation due to quantization noise in fractional-N synthesizer.

In a fractional-N synthesizer, quantization noise from Σ-Δ also degrades the modulation performance. The BER for a closed-loop modulation with a rate of 1 Mb/s is plotted against loop bandwidth in Fig. 4 for a third-order Σ-Δ modulator running at 55 MHz. As the loop bandwidth gets smaller, the effect of quantization noise is reduced. It is seen that a loop bandwidth of less than 500 kHz has little effect on the BER.

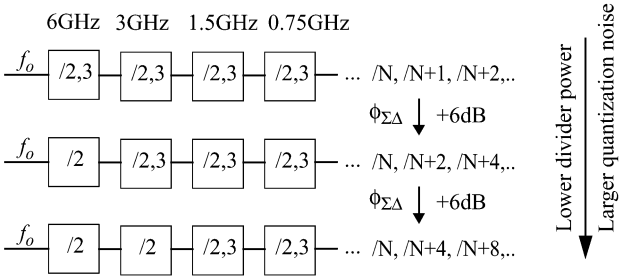

Fig. 5. Multimodulus divider architectures.

III. Low-Power Frequency Synthesizer

A. Divider versus Σ-Δ

The power consumption and noise of a Σ-Δ fractional-N synthesizer can be represented by

$$P_{\text{total}} = P_{\text{VCO}} + P_{\text{DIV}} + P_{\Sigma\Delta} + P_{\text{CPPFD}} \simeq P_{\text{VCO}} + P_{\text{DIV}} + P_{\Sigma\Delta} \quad (2)$$

$$\Phi_{\text{total}} \simeq f_{\text{VCO}}(\omega_c)\Phi_{\text{VCO}} + f_{\Sigma\Delta}(\omega_c)\Phi_{\Sigma\Delta} + f_{\text{CPPFD}}(\omega_c)\Phi_{\text{CPPFD}} \quad (3)$$

where $\Phi_{\text{VCO}}, \Phi_{\Sigma\Delta}$, and Φ_{CPPFD} are the phase noise of the VCO, quantization noise of the $\Sigma\Delta$, and noise from the charge pump and phase frequency detector (CPPFD), respectively, $f_{\text{VCO}}(\omega_c), f_{\Sigma\Delta}(\omega_c) f_{\text{CPPFD}}(\omega_c)$, is the transfer function seen by the VCO, Σ-Δ and CPPFD when the loop bandwidth of the PLL is ω_c.

In most cases, the power consumption is dominated by three components: VCO, divider, and Σ-Δ. When reducing the power consumption of these components, great care must be taken in order not to increase the output noise, since power often has direct impact on noise performance.

In the gigahertz regime, the power consumption of the frequency synthesizer is often dominated by the multimodulus dividers, especially in the first few stages where operating frequency is very high [5], [9]. Examples of multimodulus divider architectures are shown in Fig. 5. From the standpoint of power consumption, fixed prescalers are more desirable than a multimodulus divider, since multimodulus dividers require digital logic that operate near the carrier frequency and consume much more power. Therefore, power consumption can be reduced if fixed prescalers are used at the first few stages of the divider chain and the multimodulus dividers are moved to the later stages with a lower operating frequency. The penalty, however, is that the quantization noise from the Σ-Δ will increase by 6 dB each time a divide-by-two prescaler is inserted.

The noise and power consumption by the Σ-Δ can be characterized by

$$\Phi_{\Sigma\Delta}(f) = (2\pi E)^2 12 f_{\text{ref}} \left\{ sin\left(\pi \frac{f}{f_{\text{ref}}}\right)\right\}^{2(m-1)}$$
$$P_{\Sigma\Delta} \propto m f_{\text{ref}} \quad (4)$$

where f_{ref} is the clock frequency, m is the order of the Σ-Δ, and E accounts for the increase in quantization noise due to the number of prescalers in the divider chain. It can be seen that the power consumption is proportional to the clock frequency and the order of the Σ-Δ and that the output quantization noise is inversely proportional to the power consumption. Therefore, in order to reduce the increased quantization noise from prescalers, the power consumption of the Σ-Δ must be increased. Hence, there is a tradeoff between the divider and the Σ-Δ power consumption. As we try to decrease the divider power consumption by inserting fixed prescalers at high frequency stages, we lose the noise level that need to be overcome by increasing the power consumption of the Σ-Δ. A circuit level simulation which shows this tradeoff has been conducted and the results are shown in Fig. 6, where power consumption of the divider and Σ-Δ is plotted versus number of prescalers. In order to keep the total output noise given by (3) below the specification with more number of prescalers, complexity of the Σ-Δ is increased by varying the order (m) and the clock frequency. It can be seen that the total power consumption reaches a minimum when a fixed prescaler of divide-by-8 is used before a dual modulus divider.

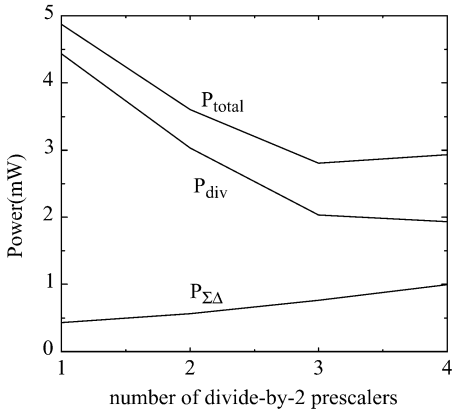

Fig. 6. Power consumption of divider and Σ-Δ.

B. Low Building Blocks

1) VCO: The VCO is based on a spiral inductor with $-g_m$ from the PMOS and the NMOS pairs as shown in Fig. 7. While many combinations of *LC* tank exist at 6.5 GHz, it is advantageous to use a small inductor and a large capacitor, since it is easier to implement smaller value high Q inductors at high frequencies. The implemented VCO uses NMOS devices that is two times larger than the minimum length device for lower $1/f$ noise.

The direct VCO modulation architecture requires two control inputs for the VCO, one for the main control from the PLL and the other for modulation. These control inputs are implemented using NMOS varactors optimized for high Q and wide tuning range [3]. The linear tuning range of the modulation varactor determines the maximum data rate.

2) Divide-by-112/120: The divide-by-112/120 is composed of three high frequency prescalers and a dual modulus divider. The prescaler-by-8 is based on high-speed divide-by-2 flip-flops as shown in Fig. 8, [10], [11]. In order to operate these dividers at a low supply voltage of 1.6 V with small input amplitude, the

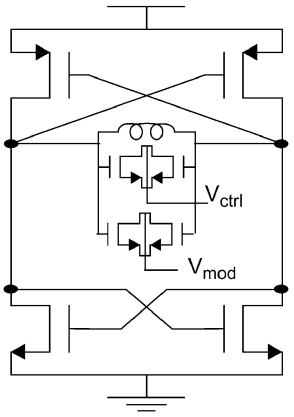

Fig. 7. Schematic of 6.5-GHz VCO.

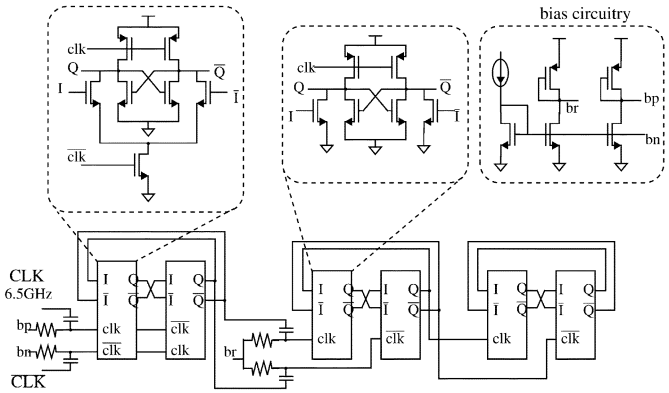

Fig. 8. Divide-by-8 prescaler.

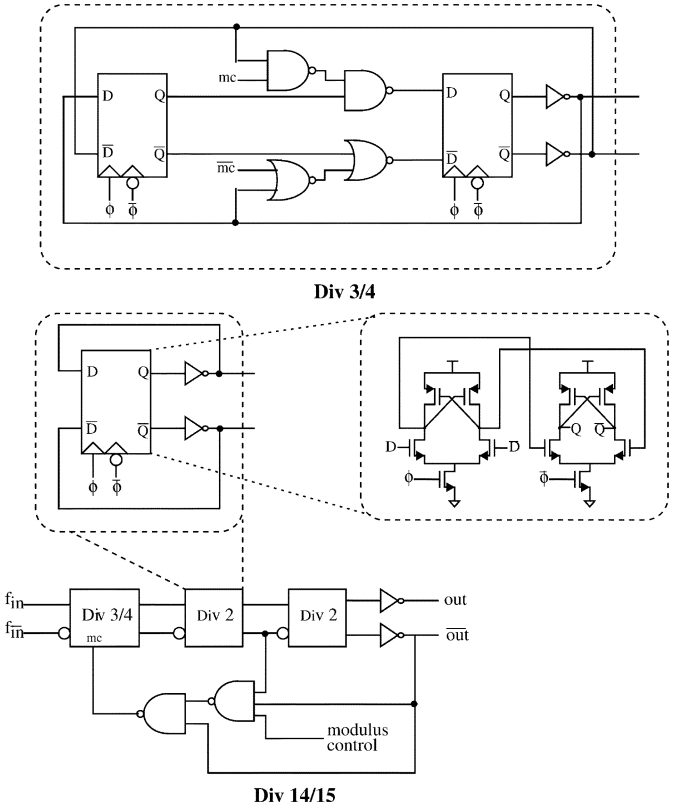

Fig. 9. Schematic of the divide-by-14/15.

Fig. 10. In order to save power, a shutdown switch S turns off the power of the variable loop charge pump when the loop is in lock.

input clocked transistors are biased separately from the input VCO signals with ac coupling capacitors. The coupling capacitors are implemented using MIM capacitors and the bias is fed through a poly resistor. The values of the capacitors and the resistors are chosen such that the input VCO signal undergoes little attenuation and such that the output noise is not affected by the thermal noise of the resistors. While the first prescaler achieves higher operating frequency, the next two prescalers have less clock capacitance and provide larger output swing necessary for the input of the divide-by-14/15 stages. The divide-by-14/15 stage is shown in Fig. 9. It is composed of a divide-by-3/4 followed by a cascade of two divide-by-2 circuits. Test results from the fabricated chip show power consumption of 3.2 mW for the divide-by-112/120 at 1.6 V, where approximately 2 mW of power is consumed in the prescaler-by-8.

3) Σ-Δ, PFD, and Charge Pump: The Σ-Δ is based on a single loop architecture rather than a MASH architecture. The single bit output of the single loop architecture allows a simple dual modulus divider compared to a multimodulus divider required by a MASH. In addition, the smaller phase difference produced by single loop Σ-Δ is better suited for loop switching, as will be seen in the next section.

The PFD is based on a popular flip-flop structure used in many PLLs [12], [13]. The dead zone is avoided by allowing enough delay through the OR gate so that current flows through the charge pump even for small phase differences. The charge pump is based on a current steering switch [14] as shown in

IV. Fast Startup Technique: Variable Loop Bandwidth

The most critical issue in sensor communication is the startup time of the transmitter, which dominates energy consumption in short packet transmission.

A. Variable Loop Bandwidth in a Fractional-N Synthesizer

In order to achieve fast startup transient with low loop bandwidth, a loop switching method is used [15], [13], [12]. To allow minimal disturbance on the VCO control voltage during switching, resistive component of the loop is changed by turning off the current source and opening the resistor paths. In addition, the loop parameters are set such that the phase margins are kept the same during loop switching.

The variable loop bandwidth technique works well in integer-N synthesizers or clock recovery PLLs, where phase error is zero when the PLL is in lock [12], [13]. Unfortunately, the phase error does not become zero for a fractional-N synthesizer even in locked condition, since the divider value is constantly changed. This nonzero phase error results in quantization error on the VCO control voltage in locked conditions. The quantization noise on the VCO control voltage can be a serious problem when loop switching is employed, especially when there is a large difference in switched loop bandwidths. Suppose the loop switches from a large bandwidth to a small bandwidth after the PLL is locked. Since the VCO control

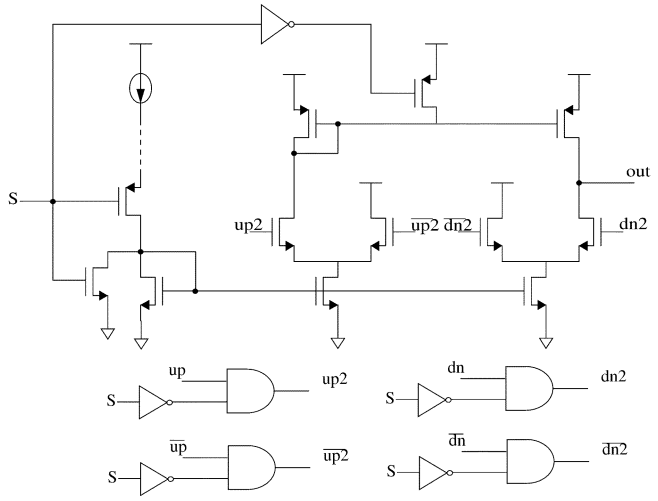

Fig. 10. Charge pump of the variable loop frequency synthesizer.

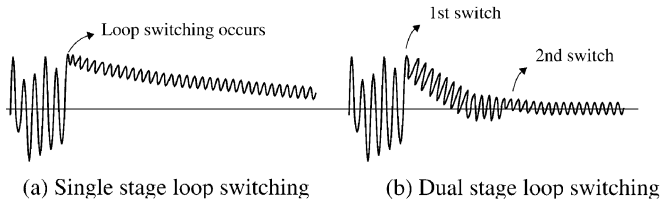

Fig. 11. Effect of quantization noise in loop switching.

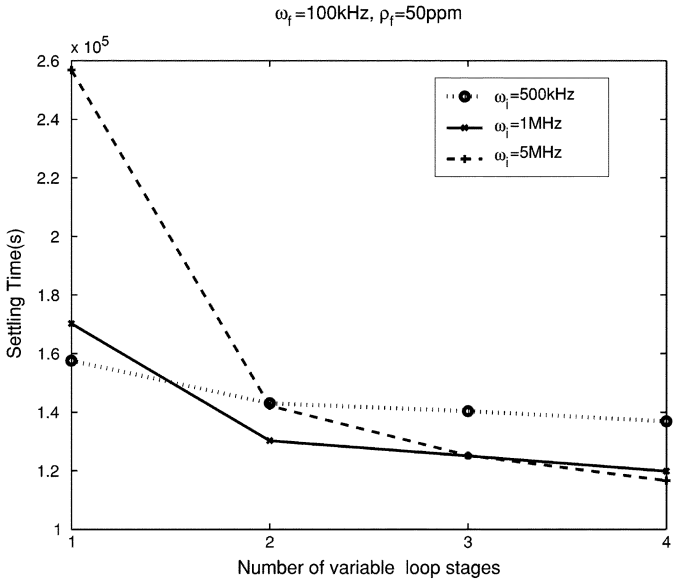

Fig. 12. Settling time versus number of variable loop stages.

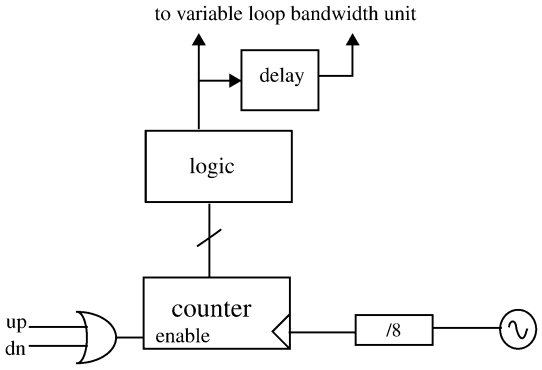

Fig. 13. Digital lock detector.

voltage fluctuates around a desired average value, the loop switching may occur at an instant when the control voltage is far away from the desired value as shown in Fig. 11(a). In such cases, the settling time is dominated by the settling time of the small loop bandwidth and the loop switching technique does not help the fast settling of the synthesizer. This problem can be alleviated if the loop switching is applied in multiple stages as shown in Fig. 11(b) [16]. By changing the loop bandwidth to an intermediate value, the magnitude of the quantization noise can be reduced and the settling time in the small loop bandwidth can be reduced.

B. Multiple Stage Loop Switching

In order to obtain the optimum number of loop switching and the values of loop components for each stage, the behavior of the VCO control voltage in multistage loop switching method is analyzed and the results are shown in Fig. 12, where minimum settling times are plotted against the number of variable loop stages for different initial loop bandwidths. The graphs shows that the settling time decreases as the number of stages increases, since each stage minimizes the effect of quantization noise. Ideally, settling time will be minimized by maximizing the number of stages, M. However, keeping M to a minimum is desirable from the implementation standpoint since addition of a variable loop stage requires increased complexity in charge pump and loop filter. Keeping this in mind, $M = 2$ with initial loop bandwidth (ω_i) of 1 MHz is appropriate for the scenario when the final loop bandwidth (ω_f) is 100 kHz and settling accuracy (ρ_f) is 50 ppm. More number of stages provides little improvement in settling time while adding circuit complexity. The graph also confirms that multistage switching is more effective when the difference between initial and final loop bandwidth is large. When the loop bandwidth starts from 5 MHz and jumps directly to 100 kHz, the settling time is large because it is dominated by the loop behavior of the small loop bandwidth. However, addition of another variable loop stages immediately reduces the settling time.

C. Digital Lock Detector

In order to detect lock, the phase difference is monitored by a digital counter located at the output of the prescaler-by-8 as shown in Fig. 13. The counter is enabled when the up or down signal from the PFD is high, i.e., when there is phase difference. Basically, the counter counts the number of high frequency pulses from divide-by-8 during the phase difference of the reference clock and the divided output of the synthesizer. The output of the counter represents the quantized value of the phase difference which decreases as the loop approaches lock. The lock is detected if the counter output is kept below a certain threshold for a period of time that corresponds to the loop bandwidth. The output of the lock detector is then fed to the variable loop bandwidth unit.

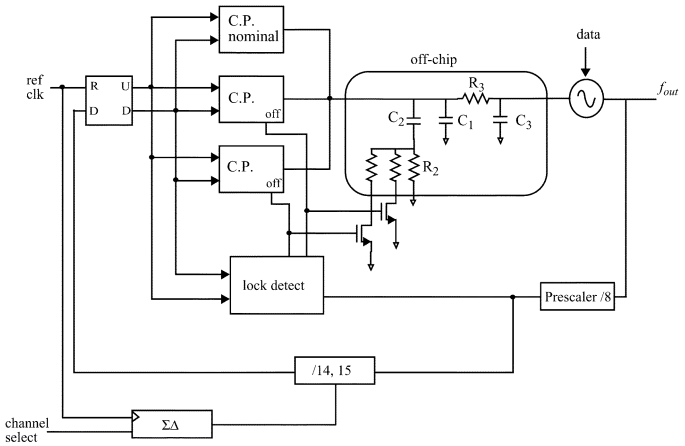

Fig. 14. Variable loop bandwidth frequency synthesizer.

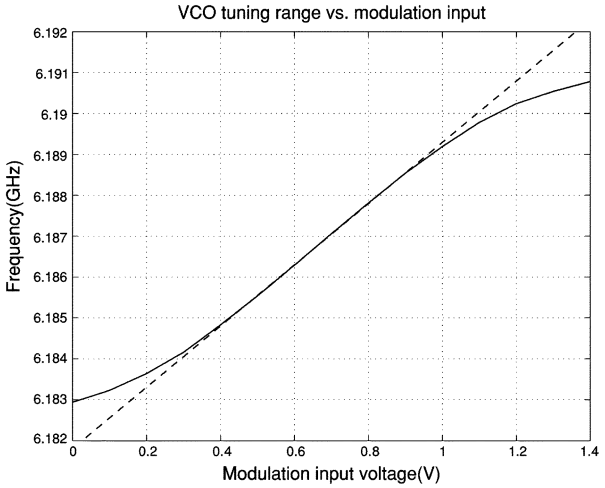

Fig. 15. Tuning characteristic of the VCO on modulation input.

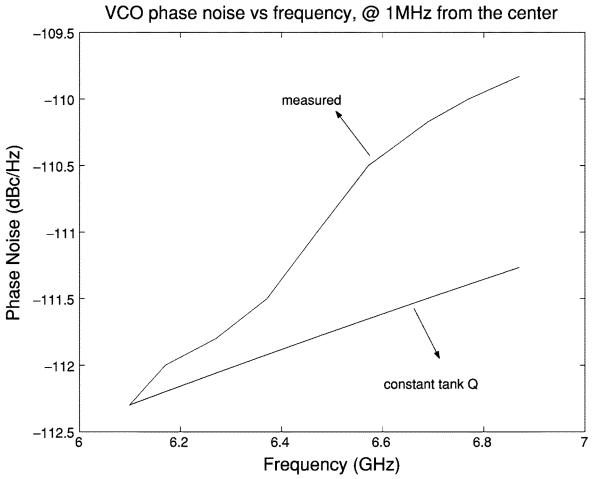

Fig. 16. Phase noise at different frequencies.

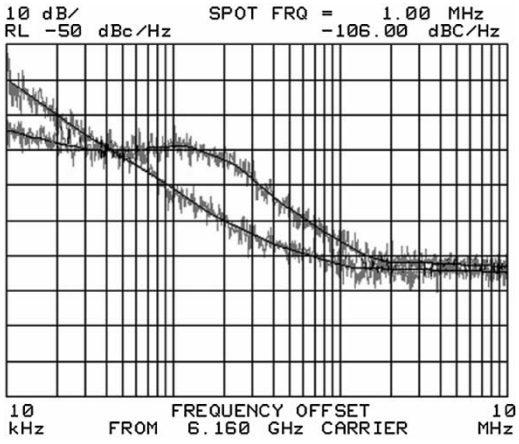

Fig. 17. Phase noise plot of the synthesizer.

V. Experimental Results

A. Energy Efficient BFSK Modulator

The block diagram of the implemented energy efficient BFSK modulator is shown in Fig. 14. The design methodologies discussed in the previous sections are applied to a prototype chip fabricated in IBM's 0.25-μm SiGe BiCMOS technology. The implemented chip uses only the CMOS part of the technology to test the capability of CMOS at high frequencies. The frequency synthesizer is able to change its frequency in about 1-MHz steps with a 55-MHz reference clock. The total power consumption of the synthesizer is 22 mW, where VCO draws 7.7 mA of current from 2.3-V power supply, while the rest of the synthesizer draws 2.7 mA from 1.6 V. The divide-by-112/120 consumes 3.2 mW, where 2 mW is dissipated is in the prescaler divide-by-8. The PFD, charge pump, and the lock detector consume 500 μW.

The VCO's center frequency is at 6.5 GHz and the tuning range is 12% (6.1 GHz–6.9 GHz). The VCO has phase noise of -112 dBc/Hz at 1-MHz offset and the $1/f$ noise is approximately 120 kHz, which is significantly lower than a single NFET's $1/f$ noise corner of couple of MHz. The phase noise variation over the tuning range is plotted in Fig. 16. It shows the measured phase noise and the ideal phase noise with constant tank Q. The ideal phase noise assumes that the the Q of the tank is constant throughout the tuning range with the value at 6.1 GHz. The degradation in phase noise with increase in operating frequency is due to the degradation of Q of the LC tank.

The tuning characteristics of the low gain varactor for the modulation input is shown in Fig. 15. It has similar curve as the large gain varactor, except that its turning range is 8 MHz. The linear tuning range of 3.5 MHz determines the maximum achievable data rate.

The output phase noise of the synthesizer is shown in Fig. 17, where the VCO phase noise is also plotted. It can be seen that the output noise of the synthesizer is higher than the VCO phase noise due to Σ-Δ and charge pump.

The eye diagram and the spectrum of the 5-Mb/s Manchester encoded data are shown in Figs. 18 and 19, respectively. The eye was measured at one eighth the carrier frequency and the peaks that are seen in the spectrum are due to Manchester encoding.

The startup times of the modulator are shown in Figs. 20 and 21, for the cases of variable and fixed loop bandwidth scheme, respectively. In the variable loop bandwidth scheme, the loop bandwidth is switched from 1 MHz to 250 kHz before it is changed to the final loop bandwidth of 100 kHz. It can be seen that the startup time of the variable loop bandwidth scheme is about 20 μs demonstrating a factor of 4 reduction compared

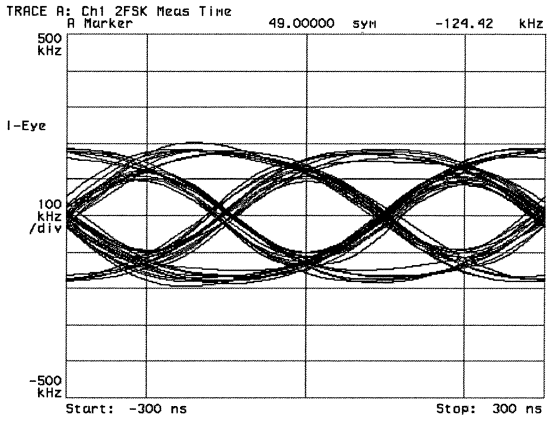

Fig. 18. Eye diagram of the 5-Mb/s Manchester encoded data.

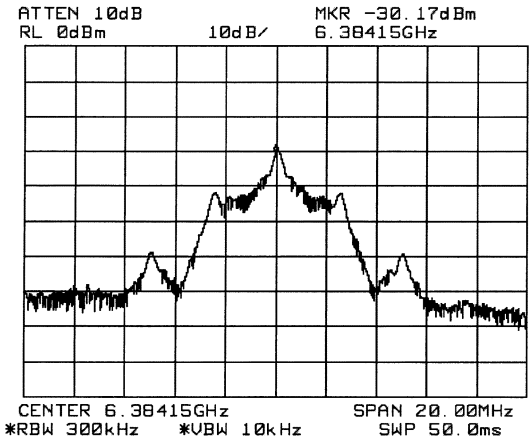

Fig. 19. Spectrum of the 5-Mb/s Manchester coded data.

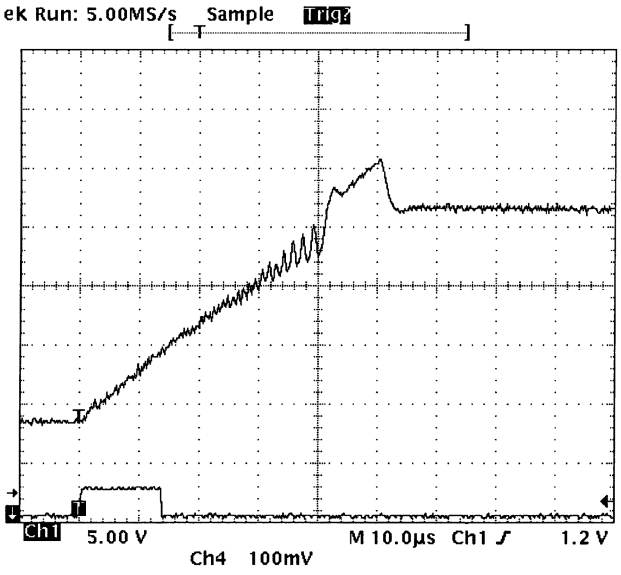

Fig. 20. Startup transient of frequency synthesizer with fixed loop.

to the fixed loop bandwidth scheme with a 100-kHz loop bandwidth.

To compare the energy efficiencies of different radios in sensor applications, we define *energy per bit* as the energy it takes to transmit a bit when sending a packet, which includes the startup energy of the transmitter. The comparison

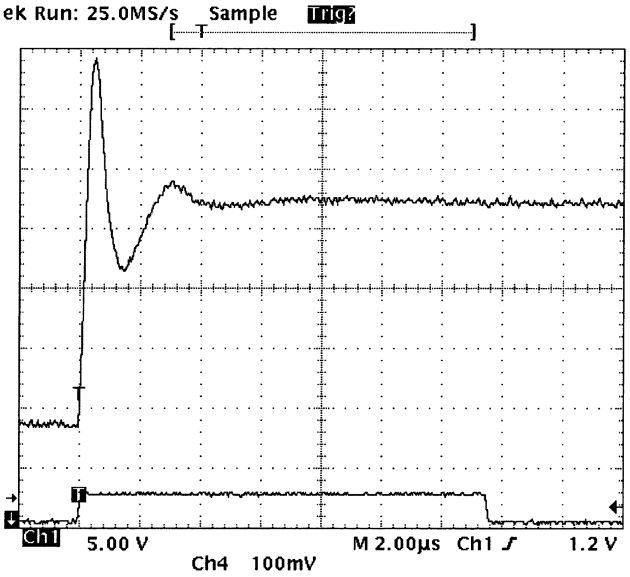

Fig. 21. Startup transient of variable loop frequency synthesizer.

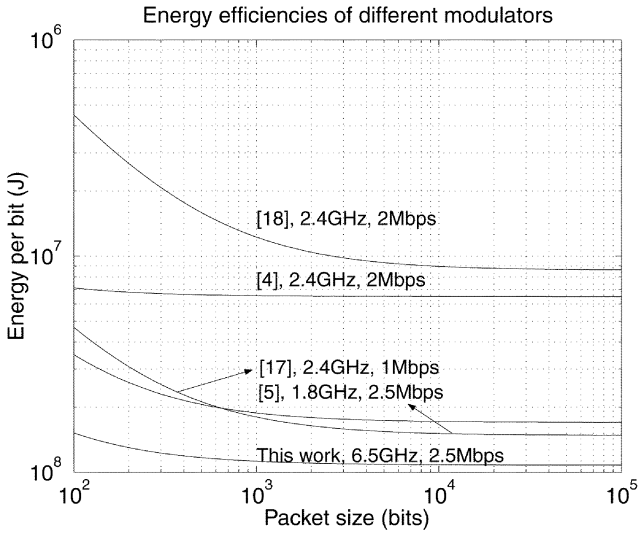

Fig. 22. Energy efficiency comparison

is shown in Fig. 22, where energy efficiencies of low-power high-data-rate radios are plotted versus packet size. It can be seen that reducing the startup time is crucial in energy efficiency for short packet transmission.

VI. Conclusion

An energy-efficient FSK modulator for wireless sensor application was implemented. Rather than just focusing on the circuit elements, the design takes into account the higher level system issue such as startup time and hence, provides an energy efficient solution suitable for the wireless microsensors. The modulator employs two-stage variable loop technique for fast startup time and direct VCO modulation for high data rate. It also exploits tradeoffs between the Σ-Δ and the divider of the synthesizer to reduce the power consumption.

There are some improvements that can be made to the implemented modulator to overcome its current drawbacks, so that it can be used in more general applications with larger

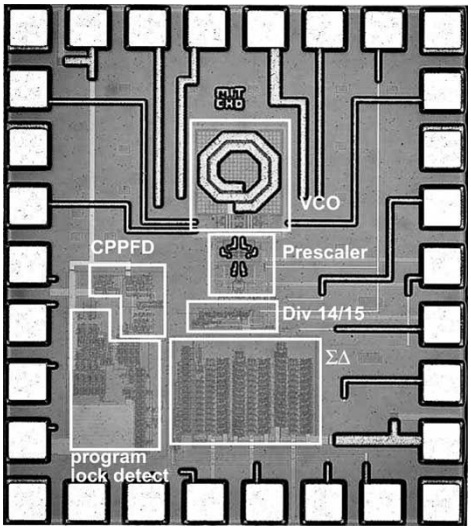

Fig. 23. Die photo of the chip.

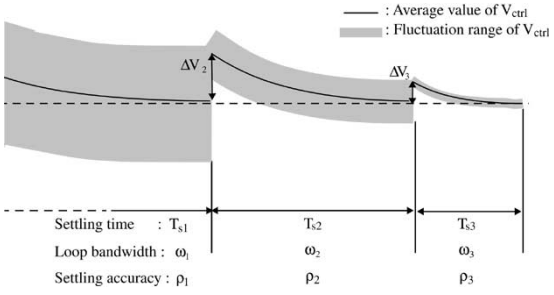

Fig. 24. VCO control voltage in multistage variable loop bandwidth technique.

power budget. First, there is the modulation error which results from VCO gain error from the modulation input. This can be overcome by applying automatic calibration circuitry as shown in [6]. Second, there is the modulation error resulting from closed-loop PLL. This can also be cancelled through a calibration circuitry [17] or cancelled at the base station's receiver by applying the inverse transfer function of the transmitter PLL.

APPENDIX
MULTIPLE STAGE LOOP SWITCHING

In order to obtain the optimum number of loop switching and the values of loop components in each stage, the behavior of the VCO control voltage in multistage loop switching method is modeled as shown in Fig. 24. The shaded region indicates the fluctuation range of VCO control voltage due to quantization noise. For a second-order PLL with an under-damped response, the error of the average VCO control voltage from the final desired value can be approximated by the following equation,

$$V_{\text{error}}(t) = \Delta V e^{-\zeta\omega_n t} \tag{5}$$

where ΔV is the difference between the final and the initial control voltage of the VCO. Hence, the time it takes to settle to within ρ accuracy of the final value, V_f, is

$$T_{si} = \frac{1}{\zeta\omega} \ln \frac{\Delta V}{\rho V_f} \tag{6}$$

For the multistage loop switching scheme, the initial voltage difference at the beginning of the ith stage can be described as,

$$\begin{aligned} \Delta V_i &= K(\omega_{i-1}^2 - \omega_i^2) + \rho_{i-1} V_f \quad i \geq 2 \\ \Delta V_1 &= V_f \quad i = 1 \end{aligned} \tag{7}$$

where K is the parameter involving loop parameters, ω_{i-1} and ω_i are the loop bandwidth of stages $i-1$ and i Hence the time it takes to settle to ρ_i of the final value V_f can be expressed as

$$T_{si} = \frac{1}{\zeta\omega_i} \ln \frac{\Delta V_i}{\rho_i} = \frac{1}{\zeta\omega_i} \ln \left(\frac{K(\omega_{i-1}^2 - \omega_i^2) + \rho_{i-1}}{\rho_i} \right)$$

The total settling time it takes for an M step variable loop switching is

$$T_{\text{settle}} = \sum_{i=1}^{M} T_{si}$$

In the above equation, only the loop bandwidth and settling accuracy of the final stage are fixed parameters (ω_f, ρ_f) and those of previous stages are variables. In addition, the number of loop stages (M) is also a variable. To obtain the optimum number of stages and loop bandwidths that minimizes the settling time, a simulation has been performed and the results are shown in Fig. 12.

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