System Design Considerations for Ultra-Wideband Communication

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ABSTRACT

This article discusses issues associated with high-data-rate pulsed ultra-wideband system design, including the baseband processing, transmitter, antenna, receiver, and analog-to-digital conversion. A modular platform is presented that can be used for developing system specifications and prototyping designs. This prototype modulates data with binary phase shift keyed pulses, communicates over a wireless link using UWB antennas and a wideband direct conversion front-end, and samples the received signal for demodulation. Design considerations are introduced for a custom chipset that will operate in the 3.1–10.6 GHz band. The chipset is being designed using the results from the discrete prototype.

INTRODUCTION

Ultra-wideband (UWB) communication is being revisited by the integrated circuit (IC) community as a medium for a high-data-rate last-meter wireless link. In 2002, the Federal Communications Commission (FCC) allowed UWB communication in the 3.1–10.6 GHz band having a –10 dB bandwidth greater than 500 MHz and a maximum equivalent isotropic radiated power spectral density of –41.3 dBm/MHz. This has triggered a large amount of interest in this area due to the promise of unprecedented wireless data rates and precise positioning in a low-cost consumer radio.

IEEE working group 802.15.3a is currently developing a high-data-rate standard utilizing the UWB band. The MultiBand OFDM Alliance (MBOA) proposal for 802.15.3a uses orthogonal frequency-division multiplexing (OFDM) modulation in a bandwidth of 528 MHz [1]. It represents a very elegant solution to the multipath problem that appears in UWB systems. On the other hand, it requires either more stringent linearity than a pulsed UWB system or the presence of a coding scheme. The direct sequence (DS-UWB) proposal for 802.15.3a communicates using pulses with a bandwidth of 2.1 GHz modulated using binary orthogonal keying [2]. For similar performance, this amounts to similar complexity and power dissipation in the receivers for pulsed and OFDM UWB systems. However, the pulse generator in a pulsed UWB transmitter may be much lower-complexity and -power than an OFDM transmitter, which requires an inverse fast Fourier transform (IFFT) operation, high-speed digital-to-analog conversion (DAC), and more linearity in the radio frequency (RF) path. Transceivers for an MBOA and a pulse-based system have recently been reported [3, 4].

This article discusses system considerations for designing a pulsed UWB system. A modular discrete prototype is presented as a platform for developing these specifications and testing custom hardware in a complete system. Some examples are shown of how the prototype may be used to achieve these goals. Finally, design considerations are introduced for a custom pulsed UWB chipset currently under development. This transceiver communicates in 528 MHz channels in the 3.1–10.6 GHz band via binary phase shift keyed (BPSK) pulses. It is being developed with the aid of the discrete prototype platform for experimental verification of the baseband algorithms and custom ICs as they become available.

UWB SYSTEM CONSIDERATIONS

Designing a UWB transceiver has several challenges, some of which are not shared with more traditional narrowband systems. This section discusses the challenges that affect the design of a custom pulsed UWB architecture. Each bit of information is encoded in the sign of a pulse (BPSK), which is then upconverted to the UWB band by multiplication with a carrier frequency. Some of the considerations addressed in this section also apply broadly to UWB systems in general.

The requirement for maximum total power consumption set by the 802.15.3a specification at 110 Mb/s and 200 Mb/s is 100 mW and 250 mW, respectively. In addition, a power save mode must be supported. To meet these constraints, a transceiver must either target the lowest power for all data rates or use an architecture that scales power with data rate. It is also advantageous to have an architecture that scales power consumption under optimal channel conditions.

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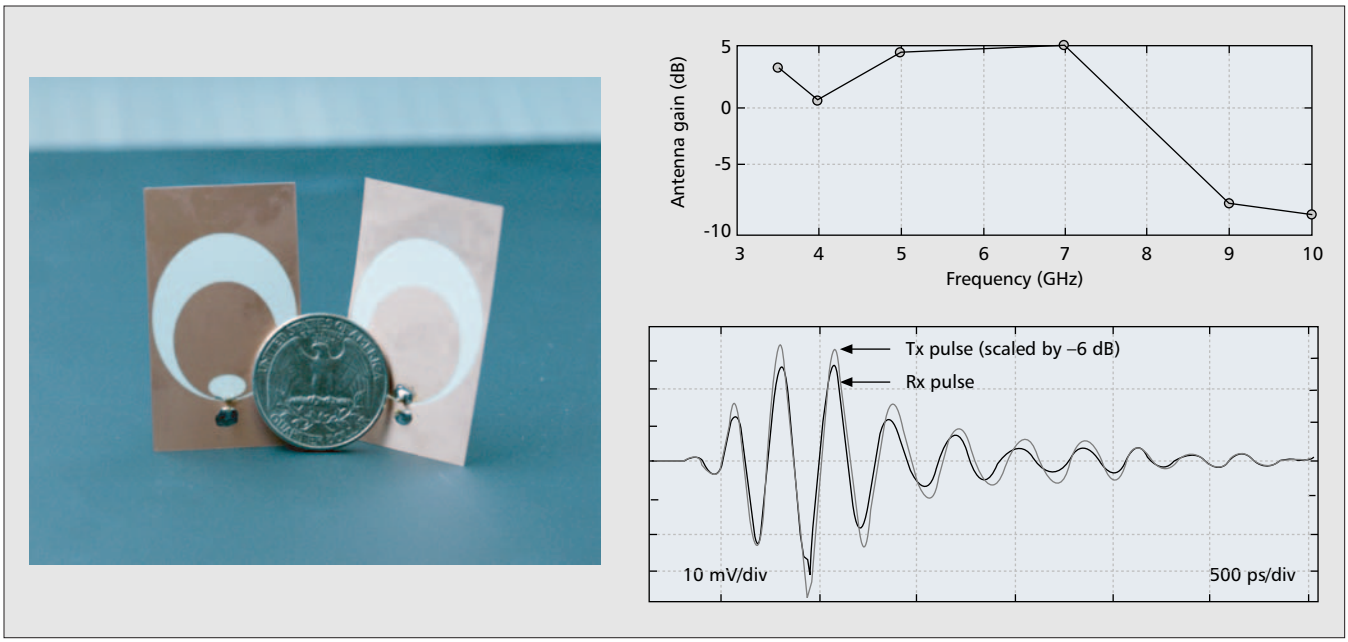

Figure 1. *UWB antenna (left) and measured antenna gain and transient response to a pulse (right) [6].*

The UWB Channel

UWB is an overlay technology and is susceptible to in-band interference from existing bands such as those used by 802.11a radios. The allowed power spectral density is low compared to narrowband systems using overlapping bands. Therefore, interference from a UWB transmitter to a narrowband receiver is arguably negligible. On the other hand, the presence of relatively large narrowband interferers in the UWB band poses very stringent constraints on the filters and linearity of the UWB front-end. For example, 802.11a radios may transmit a maximum of 16 dBm/MHz in the 5.725–5.825 unlicensed national information infrastructure (U-NII) band, and may be in close proximity to a UWB receiver. In order to cope with an 802.11a interferer at 1 m and demodulate a desired UWB signal at 10 m, it is necessary to provide an interference attenuation of 65 dB if no filtering is used in the digital baseband. To coexist with this large interferer, UWB systems typically filter and do not use the U-NII band.

A long channel impulse response is caused by severe multipath and results in intersymbol interference (ISI). This limits the symbol rate for a pulsed system, or forces very complex compensation techniques. UWB systems have excellent multipath time resolution due to the large bandwidth, and this information may be used to better compensate for the effects of multipath. For the purpose of simulating a system, the 802.15.3a working group proposed the use of a modified Saleh-Valenzuela channel model in the 3.1–10.6 GHz band [5]. The model ranges from 4 m with line-of-sight to extreme non-line-of-sight with an RMS delay spread of 25 ns.

Antenna Modeling

UWB antennas present designers with new opportunities and challenges as a UWB antenna must exhibit a nearly omnidirectional radiation pattern for a wide range of frequencies, a wideband impedance match, a linear phase response (i.e., constant group delay), and a compact profile. The wideband frequency response can be achieved by exponential tapering between the radiator and ground plane, similar to a circular disc monopole antenna. The gradual tapering allows for minimal characteristic impedance variation as the antenna moves from one resonant mode to another. A planarized version of the circular disc antenna has been designed, fabricated, and characterized. Figure 1 shows the small profile of the fabricated antenna [6]. This antenna exhibits a voltage standing wave ratio (VSWR) ≤ 2 for the entire UWB frequency range, and has exhibited a flat measured gain response for approximately an octave of frequency within the UWB frequency band, as shown in Fig. 1.

Another important point of interest with regard to UWB antenna performance is that of the time domain response. Reliable transmission and reception of a 3.1–10 GHz UWB pulse requires approximately constant group delay. This antenna exhibited comparable phase and group delay response to that of a commercial horn antenna rated for use within the 1–18 GHz frequency range [6]. A test setup was designed to exhibit the time domain performance and distortion effects of the antenna on the transmitted pulse. This included a commercial impulse generator with energy up to 10 GHz, connected to a high pass filter with a cutoff frequency of approximately 3 GHz. This signal was then passed through a wideband commercial amplifier and transmitted through the antenna. This signal was received 1 m away and measured on an oscilloscope directly at the antenna terminals [6]. The time domain measurement of the received pulse superimposed on the transmitted pulse is shown in Fig. 1, and shows qualitatively that there is very little distortion imposed by the UWB antenna on the received pulse.

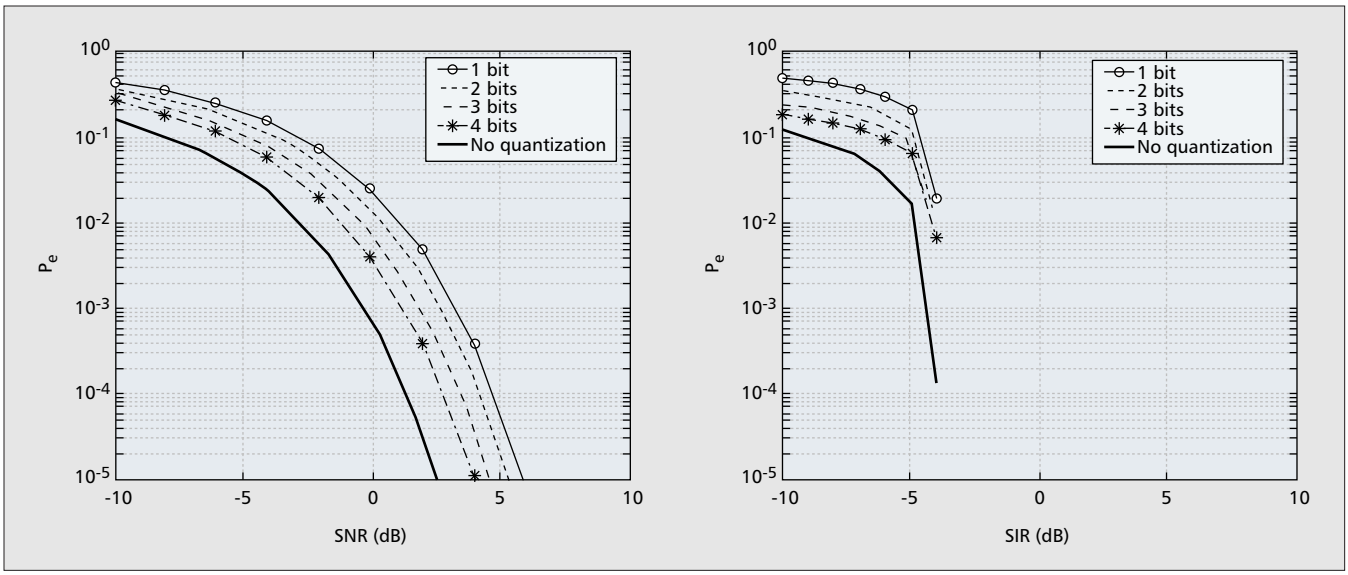

Figure 2. *Probability of error for pulsed UWB signals in the AWGN (left) and interference (right) limited cases.*

Another important aspect in UWB system design is that of the interface between the antenna and the RF front-end. The electromagnetic (EM) simulator used in this design incorporated a feature that allowed the designer to extract a lumped-element model of the antenna, enabling a circuit designer to co-design the front-end with the antenna. Although the antenna exhibits an impedance match of VSWR ≤ 2 throughout the UWB range, it varies enough that it is useful for the circuit and system designer to know how the impedance changes. As such, system conversion gain across the entire UWB bandwidth can be better designed within some tolerance. In addition to the antenna, it is important to model the antenna-microstrip interface and microstrip-package-chip interface. These parasitic inductances and capacitances from the different interfaces can be absorbed into the filter/matching network between the antenna and circuit front-end. Time domain transient pulse responses can also be simulated with the EM simulator. With these analytical tools, it is possible to examine the advantages and disadvantages of matching [7], both through the EM simulator and through a circuit simulator with the extracted lumped-element model, so the impact on wideband noise figure and gain can be analyzed. The results can readily be implemented in the discrete prototype and verified in a system context.

RF Front-End

In this pulse-based BPSK system, each bit is encoded as a pulse with either positive or negative polarity. It is desirable to shape the transmitted pulse in order to maximize the transmit power given the spectral mask and minimize adjacent channel interference and out-of-band emissions. The Gaussian pulse has desirable time and frequency domain characteristics, and can be approximated with a simple circuit [8]. The channel estimation made in the digital baseband of the receiver relies on matched positive and negative pulse shapes, a nontrivial specification if pulses are inverted with complementary circuits (i.e., NMOS and PMOS). Mismatch in pulse shapes has a similar effect on system performance as a DC offset.

UWB transmitted power levels are required to be below that of noise emissions allowed for electronic equipment, and receiver sensitivity is therefore high. To reduce dynamic range requirements in the receiver, typical UWB frequency plans avoid the 802.11a bands. A wideband low noise amplifier (LNA) with a notch filter may be used for this architecture, but there is a trade-off between adjacent channel attenuation and the duration of the filter impulse response. A switchable 802.11a filter in the front-end allows selective use of this band for UWB communication if no interferers are present. Placing the notch filter after the LNA reduces the noise figure but increases the linearity requirements of the LNA. By using a direct conversion architecture, a very expensive intermediate frequency filter can be avoided. In order not to introduce unnecessary complexity in the demodulation, the entire RF path from transmitter to receiver must meet a very stringent constraint on the length of its impulse response, or equivalently have a constant group delay over the entire bandwidth.

Analog to Digital Converter

The ADC becomes a non-trivial part of the system as sampling rates will in general exceed 500 MS/s. A flash ADC architecture implies an exponential growth in complexity with the number of bits. Other architectures such as successive approximation register (SAR) imply a more modest growth. In addition, the input data to the digital baseband comprises samples of the real and imaginary parts of the signal, doubling the rate at which it must process the data. For example, at a sample rate of 500 Msamples/s at 5 b resolution from each analog-to-digital converter (ADC), this is a total throughput of 1 Gsample/s at 5 b. The digital baseband must be able to provide analysis at this data rate. In order to minimize power and complexity, it is important to

determine the minimum required ADC precision for reliable communication.

System performance was simulated while varying the number of bits for both the noise and interference limited cases [9]. Additive white Gaussian noise (AWGN) of the same bandwidth as the signal was considered for the noise limited case. An exponential sinusoid of a random frequency and initial phase within the signal bandwidth was considered for the interference limited case. Figure 2 shows the results of these simulations as functions of the signal-to-noise ratio (SNR) and signal-to interference ratio (SIR). The UWB signal considered was 100 Mb/s BPSK pulses at a link distance of 10 m. There is a very sharp threshold effect in the interference limited environment. This may be explained as the point at which the amplitude of the pulses is large enough that the sinusoidal interferer is not able to change the sign of the samples. The plots indicate that 4 bits are sufficient in any situation for reliable UWB demodulation. But it also shows that in several situations like the AWGN limited environment, a 1 bit ADC is sufficient. Dynamically adapting the number of bits of the ADC to the conditions of the environment can drastically downscale the digital baseband complexity and total power consumption.

Digital Baseband

The digital baseband performs packet synchronization and demodulation, and must compensate for ISI and provide automatic gain control for the front-end. A RAKE receiver may be used for boosting the received SNR. However, ISI will occur if the channel impulse response is longer than the symbol period. This may be compensated for using a Viterbi maximum likelihood sequence estimation (MLSE), whose complexity grows exponentially with the length of the impulse response. The impulse response that the baseband must compensate is comprised of the channel impulse response convolved with the impulse response of the elements that operate on the signal before being digitized (i.e., LNAs, filters).

If the UWB system is to work in WLAN conditions, the time to achieve packet acquisition is a key parameter. This directly affects the duration of the preamble of a data packet. The energy used during the detection of the preamble is a constant amount, independent of the duration of the data packet. Therefore, it is important to minimize the duration of the preamble. The complexity of locking to a pulsed signal grows with its bandwidth as the effective sampling frequency increases. This is a function of the length of the Gold code used in the preamble and its duty cycle. It should be comparable to other WLAN standards such as IEEE 802.11a, which uses a preamble of 20 μs.

Discrete Prototype

A flexible platform for prototyping a UWB system provides several advantages over simulation alone or iteration of a design in silicon. It offers the ability to program system specifications such as the pulse shape, ADC bit precision, or front-end nonlinearities, and to measure system performance and compare with simulations. System specifications may also be swept in the hardware for determining optimal settings for the realized transceiver. As individual chips such as the baseband processor, ADC, or front-end are designed, the corresponding component in the prototype may be substituted by the fabricated part. This enables testing the chip in a complete system, on top of verifying that the component meets its individual specifications.

Architecture

The discrete prototype is built using off-the-shelf components and commercially available test and measurement equipment. It can be divided into three distinct sections: the transmitter, the receiver, and the ADC and baseband processing. The link between the transmitter and receiver can be made through wireless transmission using various antennas [6] and spatial configurations to emulate a wide range of channels. The transmitter and receiver may otherwise be directly connected through a cable with a variable attenuator to emulate an ideal channel. A block diagram of the prototype is shown in Fig. 3, and described in more detail in the following sections.

Transmitter — The transmitter uses a direct conversion architecture to upconvert a baseband signal to a center frequency of 5.355 GHz, as shown in Fig. 3. This center frequency was chosen based on the availability of wideband RF components that operate in this range. The baseband UWB signal is generated using either a programmable arbitrary waveform generator (AWG) or a dedicated pulse generator built using off-the-shelf components. The amount of memory in the AWG limits the transmitted signal to 4 ms of data sampled at 4 Gsamples/s; however, this is long enough to store hundreds of data packets. Using an AWG enables a large amount of flexibility in the shape of the pulses transmitted, modulation scheme, and duration of transmission. For example, although this work focuses on pulse-based systems, OFDM can also be synthesized as long as a quadrature transmitter is not required. The samples for the AWG are generated using a PC and downloaded to the instrument. Various nonidealities may also be added to the signal prior to generating the samples such as gain mismatch or nonlinearity. In-band interferers such as 802.11a or random tones may also be added.

The AWG is useful for implementing one-way communication with great flexibility, but is limited in how fast new data can be downloaded to the instrument. In order to implement real-time communication, a dedicated pulse generator is used. This is built using discrete components, and generates BPSK pulses with an upconverted bandwidth of 500 MHz. A functional schematic of the discrete pulse generator is shown in Fig. 3. All logic functions were implemented using commercially available ECL components. It has a USB 2.0 interface through a field programmable gate array (FPGA) with enough local memory to store one packet of data. Once a packet has been fully buffered in the FPGA, the bits are shifted out to the pulse

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Tunable phase error is desirable in the prototype for testing the robustness of the digital baseband. This phase error can be introduced simply by tuning the RF center frequency away from 5.355 GHz.

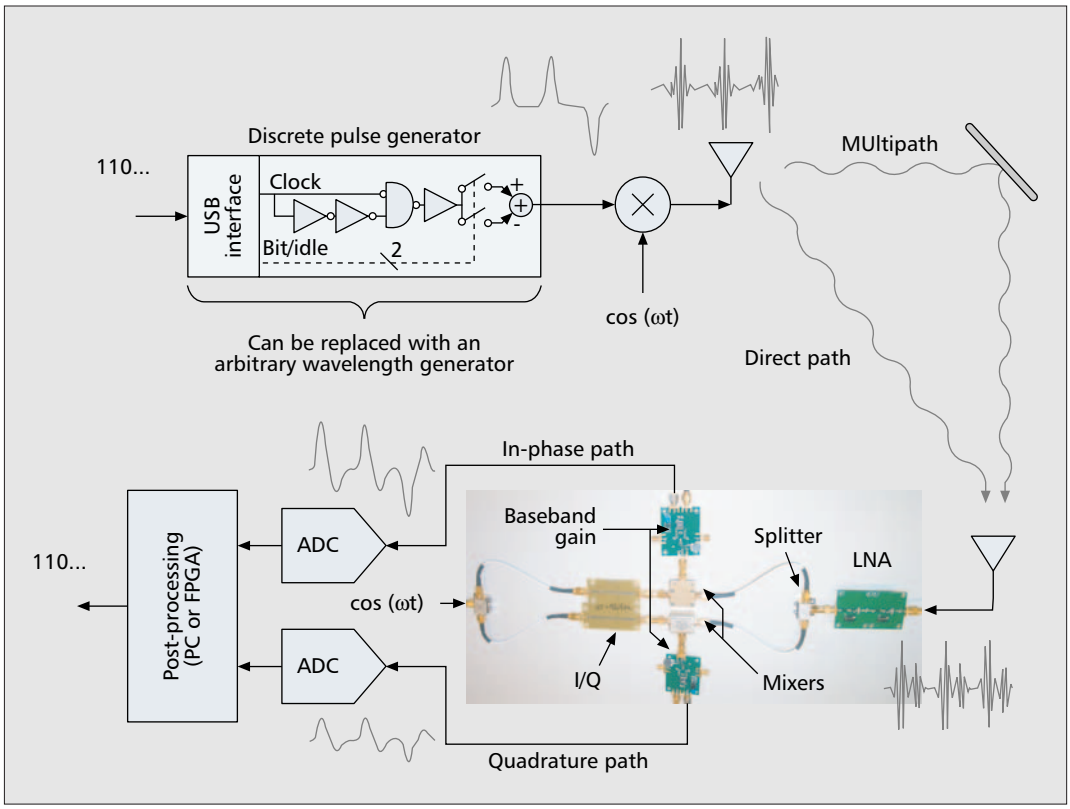


Figure 3. *Block diagram of the discrete prototype.*

generator and transmitted at 50 Mb/s. The pulse shape is fixed in the dedicated pulse generator; however, a variable pulse repetition frequency (PRF) up to 50 MHz is supported, limited by the speed of the analog switches used. The system is capable of a 100 MHz PRF when the AWG is generating the baseband pulses.

Receiver — The RF front-end is built entirely using discrete components. As shown in Fig. 3, the received signal is amplified by two cascaded LNAs, then split and applied to two identical passive mixers performing I/Q direct conversion. The 90° phase shift in the local oscillator (LO) is implemented by fixed, unequal delays in the LO transmission lines to each mixer. This method of phase shifting provides quadrature tones at 5.355 GHz, but also allows for tuning of the I/Q phase error simply by tuning the RF center frequency. Tunable phase error is desirable in the prototype for testing the robustness of the digital baseband. After I/Q downconversion, the baseband signals are filtered and amplified with an adjustable gain before being digitized.

ADC and Baseband Processing — The baseband I and Q signals from the front-end are sampled by a dual-channel 8-bit 500 Msamples/s ADC board that interfaces to a PC directly through the PCI bus. The full-scale voltage, sample rate, and capture record length are all adjustable. The received samples are buffered and captured to a file for post-processing and demodulation. Once the samples are captured to a file, virtually any baseband algorithm not requiring real-time control of the system may be tested. This includes acquisition and fine tracking, channel estimation, interferer rejection, and demodulation. Feedback loops such as automatic gain control require real-time sampling, and therefore cannot be tested using this acquisition board. An implementation on an FPGA has been demonstrated that provides basic real-time demodulation.

Range of Applicability

Several of the concepts developed in the previous sections may be tested using the prototype. For example, the trade-off between quality of service and signal processing complexity may be evaluated, and how this trade-off depends on the channel quality. Figure 4 shows a plot in which the impact of the number of bits used to represent the channel impulse response is plotted for two different channels. On the top curve, an isotropic antenna [6] is used that allows multipath to be captured (similar to an antenna that a WPAN device would use). The duration of the impulse response measured with this antenna is 20 ns, which includes echoes from reflectors in the channel. A decrease in the probability of error is obtained as the number of bits of the representation of the channel increases. The low SNR of this channel emphasizes this effect. The lower curve represents the case in which both transmitter and receiver are using a directional horn antenna with 13 dB of gain in the direct path and no significant echoes. The higher SNR combined with the presence of only a clear direct path makes the performance for this kind of channel independent of the number of bits used to represent the channel impulse response. Both

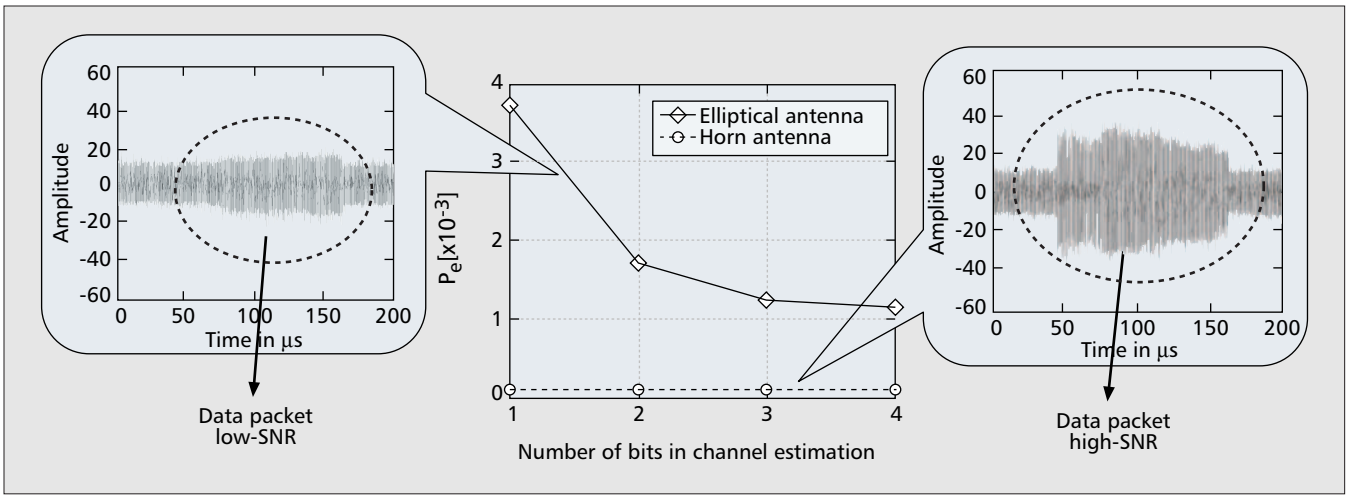


Figure 4. *Effective probability of error for transmission with two different antennas measured using the discrete prototype.*

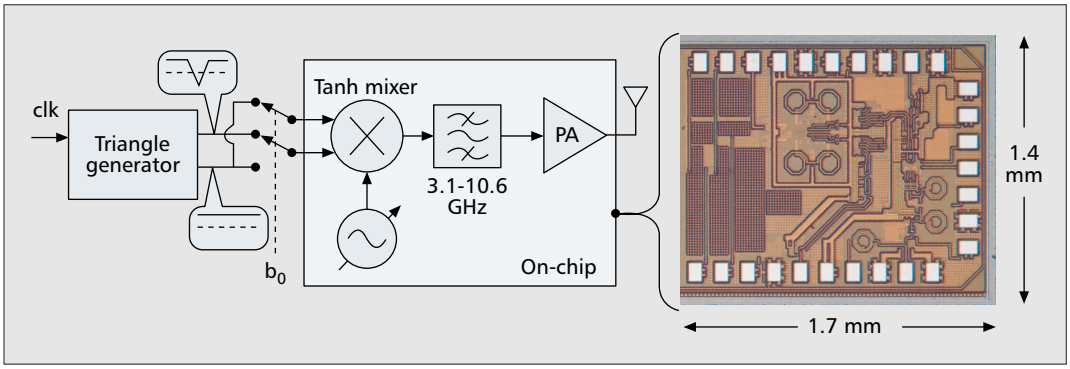


Figure 5. *Block diagram and die photo of the custom pulse generator.*

curves were obtained using measured data and a Viterbi MLSE of four states. The presence of the Viterbi MLSE improved the performance of the transceiver by reducing bit errors in the multipath channel.

These two experiments show that it is possible to trade off complexity of signal processing with quality of service, but this trade-off is only relevant if the channel quality is known. For some situations it is possible to reduce the complexity of the signal processing to the minimum.

Next-Generation Transceiver

The prototype is being used to aid in the development of a chipset for a UWB transceiver with a similar architecture that operates in the 3.1–10.6 GHz range and targets a 100 Mb/s data rate at 10 m. This transceiver communicates via BPSK modulated pulses at a maximum PRF of 100 MHz. The baseband pulse train is upconverted to one of 14 528 MHz channels in the 3.1–10.6 GHz band. This frequency plan has been adopted from an 802.15.3a proposal [1]. Fast frequency hopping between channels is not implemented in this chipset; however, it could be adopted in future revisions because of the architecture used. As the components of the system are designed and fabricated, they can be individually substituted into the prototype to verify overall system functionality.

Pulse Generator

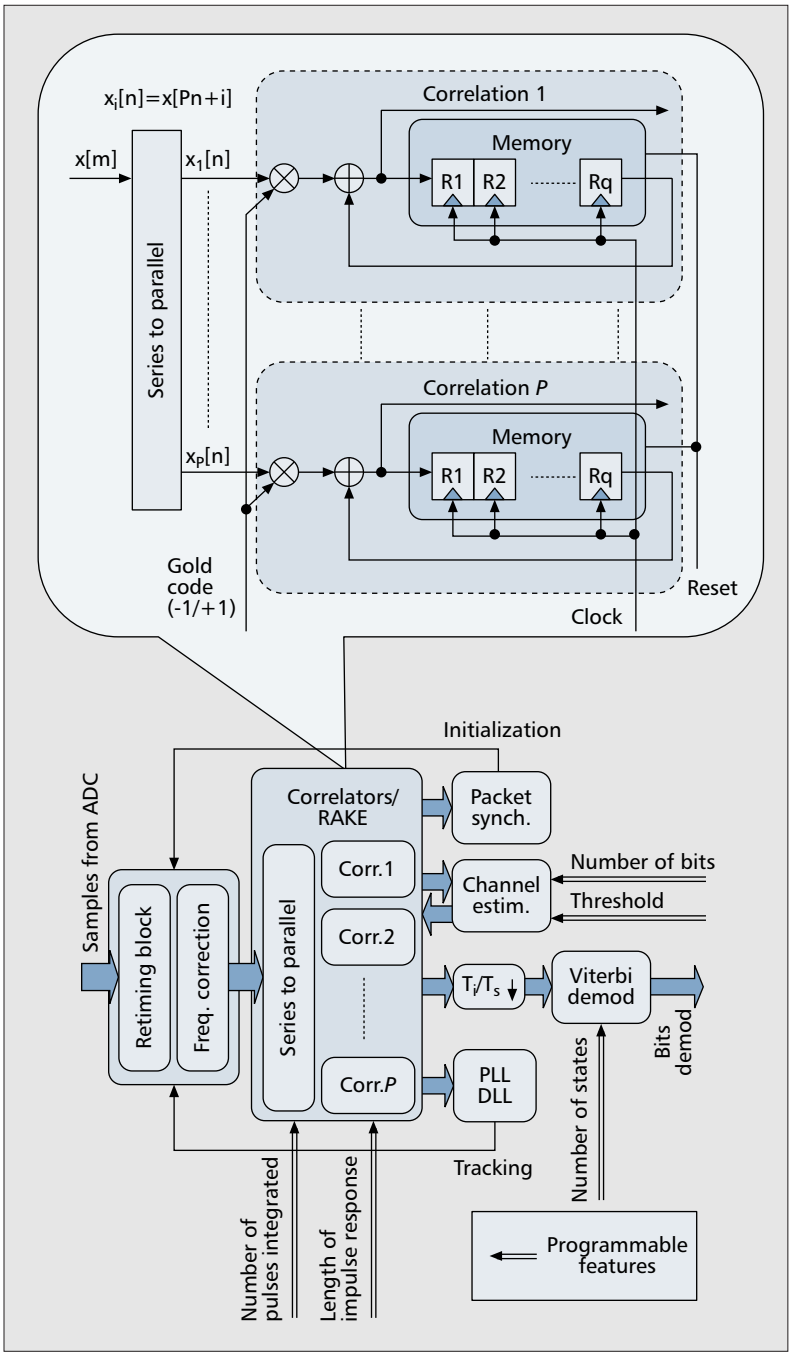
A custom pulse generator has been fabricated in a 0.18 µm SiGe BiCMOS process [8]. It generates approximate Gaussian pulses by exploiting the *tanh* voltage-current relationship of a differential pair of BJTs. The pulses are simultaneously shaped and up-converted to one of the 14 channels in the UWB band by modulating the bias current of the differential pair with a carrier frequency. BPSK pulses are generated by inverting the carrier as opposed to inverting the baseband pulse. This results in better matching between BPSK pulses. A block diagram of the transmitter is shown in Fig. 5. The pulses are triggered by a triangle-shaped signal generated off-chip. The carrier frequency is generated on-chip by an LC voltage controlled oscillator (VCO) or from an external local oscillator (LO). The output of the pulse-shaping mixer is an upconverted pulse centered around the carrier frequency. This signal passes through a band-select filter and amplifier, then off-chip to the UWB antenna. A die photo of the chip is shown in Fig. 5.

Baseband Processing

The digital baseband is being designed in complementary metal oxide semiconductor (CMOS) technology [10]. In order to reliably transmit 100 Mb/s over 10 m it is necessary to address the multipath that may affect communication in the

UWB channel. This is performed in the digital baseband using the architecture shown in Fig. 6. It includes both a RAKE receiver with a variable number of fingers and a Viterbi MLSE.

The baseband characterizes the channel quality in terms of the channel impulse response and SNR. It also exposes several knobs that allow the complexity of some of its blocks to be controlled (e.g., number of bits of the channel estimation, length of the channel impulse response, number of states of the Viterbi MLSE). Based on the channel quality, higher levels of the communication hierarchy may use these knobs to trade off quality of service with power consumption and complexity for any given channel quality conditions. The core of this baseband is a set of parallel correlators whose concept is shown in Fig. 6. More power-efficient implementations of these correlators are possible. By adjusting the number of parallel correlations performed with this core, it is possible to trade off preamble duration with probability of packet acquisition.



■ **Figure 6.** *UWB digital baseband architecture.*

SUMMARY

Several considerations have been discussed as they apply to a custom pulse-based UWB system; however, one overruling specification is power consumption. System designers should consider architectures with power scaling hooks for scaling back power when the highest performance is not required. A prototyping platform realized with discrete components and commercial test and measurement equipment has been presented that assists in the design and verification of hardware, baseband processing algorithms, and models for UWB systems. A 3.1–10.6 GHz transceiver was introduced that is targeting 100 Mb/s at 10 m. As these custom ICs become available, they can be individually demonstrated in a UWB system by substitution into the discrete prototype.

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BIOGRAPHIES

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