Basics of Low Power Circuit and Logic Design

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High Performance Processors

Microprocessor Power
(source ISSCC)

![Graph showing microprocessor power over time.](Image)
Portable Devices

Required Portable Functions

- Radio transceiver
- Modem
- Voice I/O
- Pen Input
- Text/Graphics Processing
- Text/Graphics display
- Video decompression
- Full-motion video display

How to get 8 hours of operation ??
Battery Trends

(from Jon Eager, Gates Inc., S. Watanabe, Sony Inc.)
Where Does Power Go in CMOS?

- **Dynamic or switching currents**
  - Charging and discharging parasitic capacitors

- **Short-circuit or direct-path currents**
  - Direct path between supply rails during switching

- **Leakage currents**
  - Reverse bias diode leakage
  - Sub-threshold conduction

- **Static currents**
Dynamic Power of a CMOS Gate

\[ E_{0 \rightarrow 1} = C_L V_{dd}^2 \]

\[ \int_{0}^{T} P(t) \, dt = V_{dd} \int_{0}^{T} i_{supply}(t) \, dt = V_{dd} \int_{0}^{T} C_L dV_{out} = C_L \cdot V_{dd}^2 \]

\[ E_{\text{cap}} = \int_{0}^{T} P_{\text{cap}}(t) \, dt = \int_{0}^{T} V_{out} \cdot i_{\text{cap}}(t) \, dt = V_{dd} \int_{0}^{T} C_L V_{out} \, dV_{out} = \frac{1}{2} C_L \cdot V_{dd}^2 \]
Modification for Circuits with Reduced Swing

- Can exploit reduced swing to lower power
  (e.g., reduced bit-line swing in memory)

\[ E_{0 \rightarrow 1} = C_L \cdot V_{dd} \cdot (V_{dd} - V_t) \]
Physical Capacitance of an Inverter

- Important to account for capacitive non-linearities in power estimation
Node Capacitance is a Function of Voltage

![Graph showing the relationship between switched capacitance and voltage. The graph plots switched capacitance in femtofarads (fF) against voltage (V）。 Three curves are shown: LCLR, TSPCR, and C²MOS. The x-axis represents voltage (VDD) in volts (V), ranging from 0.8 to 1.5. The y-axis represents switched capacitance in femtofarads (fF), ranging from 50 to 110. Each curve shows an increase in switched capacitance as voltage increases.](image)
Consider switching a CMOS gate for $N$ clock cycles

$$E_N = C_L \cdot V_{dd}^2 \cdot n(N)$$

$E_N$: the energy consumed for $N$ clock cycles

$n(N)$: the number of 0-$\rightarrow$1 transition in $N$ clock cycles

$$P_{avg} = \lim_{N \to \infty} \frac{E_N}{N} \cdot f_{clk} = \left( \lim_{N \to \infty} \frac{n(N)}{N} \right) \cdot C_L \cdot V_{dd}^2 \cdot f_{clk}$$

$$\alpha_{0 \rightarrow 1} = \lim_{N \to \infty} \frac{n(N)}{N}$$

$$P_{avg} = \alpha_{0 \rightarrow 1} \cdot C_L \cdot V_{dd}^2 \cdot f_{clk}$$
Factors Affecting Transition Activity, $\alpha_{0->1}$

- **“Static”** component (does not account for timing)
  - Type of Logic Function (NOR vs. XOR)
  - Type of Logic Style (Static vs. Dynamic)
  - Signal Statistics
  - Inter-signal Correlations

- **“Dynamic”** or timing dependent component
  - Circuit Topology
  - Signal Statistics and Correlations
Type of Logic Function: NOR vs. XOR

Example: Static 2 Input NOR Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Truth Table of a 2 input NOR gate

Assume:

\[ p(A=1) = 1/2 \]
\[ p(B=1) = 1/2 \]

Then:

\[ p(\text{Out}=1) = 1/4 \]
\[ p(0\rightarrow 1) = p(\text{Out}=0).p(\text{Out}=1) \]
\[ = 3/4 \times 1/4 = 3/16 \]

\[ \alpha_{0\rightarrow 1} = 3/16 \]
**Type of Logic Function: NOR vs. XOR**

Example: Static 2 Input XOR Gate

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Truth Table of a 2 input XOR gate

Assume:

\[ p(A=1) = \frac{1}{2} \]
\[ p(B=1) = \frac{1}{2} \]

Then:

\[ p(\text{Out}=1) = \frac{1}{2} \]
\[ p(0\rightarrow1) = p(\text{Out}=0).p(\text{Out}=1) = \frac{1}{2} \times \frac{1}{2} = \frac{1}{4} \]

\[ \alpha_{0\rightarrow1} = \frac{1}{4} \]
Type of Logic Style: Static vs. Dynamic

**STATIC NOR**

\[ \alpha_{0 \rightarrow 1} = \frac{3}{16} \]

**DYNAMIC NOR**

\[ \alpha_{0 \rightarrow 1} = \frac{N_0}{2^N} = \frac{3}{4} \]

Power is only dissipated when Out=0!
Another Logic Style: Dynamic DCVSL

Guaranteed transition for every operation!

\[ \alpha_{0 \rightarrow 1} = 1 \]
Influence of Signal Statistics on $\alpha_{0->1}$

$p_0 = (1-p_a) (1-p_b)$

$p_{0->1} = p_0 p_1 = (1-(1-p_a) (1-p_b)) (1-p_a) (1-p_b)$

• $\alpha_{0->1}$ is a strong function of signal statistics
Inter-signal Correlations

(a) Logic circuit without reconvergent fanout

\[ p_{0 \rightarrow 1} = (1 - p_a p_b) p_a p_b = \frac{3}{16} \]

(b) Logic circuit with reconvergent fanout

\[ p_Z = p(C=1|B=1) \cdot p(B=1) \]
\[ p_{0 \rightarrow 1} = 0 \]

- Need to use conditional probabilities to model inter-signal correlations!
- CAD tools required for such analysis
"Dynamic" or Glitching Activity in CMOS

\( \alpha_{0\rightarrow1} \) can be > 1 due to glitching!
Glitch Reduction Using Balanced Paths

Ripple

Lookahead
Comparison of Adder Topologies

<table>
<thead>
<tr>
<th></th>
<th>16 bit</th>
<th>32 bit</th>
<th>64 bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ripple Carry</td>
<td>3.09</td>
<td>0.81</td>
<td>0.27</td>
</tr>
<tr>
<td>Carry Lookahead</td>
<td>10.0</td>
<td>3.54</td>
<td>1.76</td>
</tr>
<tr>
<td>Carry Bypass</td>
<td>5.45</td>
<td>2.39</td>
<td>0.99</td>
</tr>
<tr>
<td>Carry Select</td>
<td>4.44</td>
<td>2.08</td>
<td>1.00</td>
</tr>
<tr>
<td>Conditional Sum</td>
<td>3.82</td>
<td>1.23</td>
<td>0.42</td>
</tr>
</tbody>
</table>

Logic Transition Histogram

from [Callaway92]
(VLSI Signal Processing, V)
Glitching at the Datapath Level

(A + B) + (C + D)

Tree vs. Chain

(A + B) + C + D

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Normalized # of Transitions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Tree</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
</tr>
</tbody>
</table>

- Can be reduced by reducing the logic depth and balancing signal paths
Short-circuit Component of Power

\[ V_{in} \rightarrow V_{dd} \rightarrow C_L \rightarrow V_{out} \]

\[ I_{VDD} (mA) \]

\[ 0.0 \quad 1.0 \quad 2.0 \quad 3.0 \quad 4.0 \quad 5.0 \]

\[ 0.0 \quad 0.05 \quad 0.10 \quad 0.15 \]
Short-Circuit Current vs. Load Capacitance

from [Veendrick84]

Minimizing Short-circuit Power

- Keep the input and output rise/fall times the same
  (< 10% of Total Consumption)
  (from [Veendrick84]
  *(IEEE Journal of Solid-State Circuits, August 1984)*)

- If $V_{dd} < V_{tn} + |V_{tp}|$ then short-circuit power can be *eliminated*!
Reverse Biased Diode Leakage

I_{DL} = J_S \times A

- J_S = 1-5pA/\mu m^2 for a 1.2\mu m CMOS technology
- J_S double with every 9^0C increase in temperature
Subthreshold Leakage Component

- Leakage control is critical for low-voltage operation
Static Power

\[ P_{\text{static}} = p(\text{ln}=1) \cdot V_{dd} \cdot I_{\text{stat}} \]

- Not a function of switching frequency
Ultra Low Power System Design

- **System**
  - Design partitioning, Power Down

- **Algorithm**
  - Complexity, Concurrency, Locality, Regularity, Data representation

- **Architecture**
  - Concurrency, Instruction set selection, Signal correlations, Data Representation

- **Circuit/Logic**
  - Transistor Sizing, Logic optimization, Activity Driven Power Down, low-swing logic, adiabatic switching

- **Technology**
  - Threshold Reduction, Advanced packaging

Lower Supply Voltage and Switched Capacitance
Signal Processing Attributes

- Throughput constrained computing
  - 30ms refresh rate requirement for video
  - Optimize power supply voltages

- Time-varying computational requirements
  - Adaptive signal processing techniques

- Knowledge of signal statistics

```
<table>
<thead>
<tr>
<th>Speech Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time</td>
</tr>
</tbody>
</table>

```

```
<table>
<thead>
<tr>
<th>Transition Probability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit Number</td>
</tr>
</tbody>
</table>

```

“water all year”
Energy Efficiency Metric: Fixed Throughput

Example: Video Compression

\[ P = \left( \sum (N_iC_iV_{dd}^2) \right) f_{sample} \]

Energy/Sample

\[ f_{sample} \text{ is fixed} \]

For this mode (most DSP applications), minimizing energy/sample is both Energy and Power Efficient.
Energy Efficiency Metric: Max Throughput

\[ ETR \equiv \frac{\text{Energy} / \text{operation}}{\text{Throughput}} = \frac{\text{Power}}{\text{Throughput}^2} \]

- A lower ETR (higher efficiency) indicates lower energy for constant throughput, or higher throughput for constant energy.

Other metrics such as \( E \times D \),
see [Horowitz94],
(1994 Symposium on Low-power Electronics)
Supply Voltage Scaling

Lowering $V_{dd}$ reduces energy but increases delays.

$T_d = \frac{C_L \cdot V_{dd}}{I}$

$I \sim (V_{dd} - V_t)^2$

$\frac{T_d(V_{dd}=1.5)}{T_d(V_{dd}=5)} = \frac{(1.5) \cdot (5 - 0.7)^2}{(5) \cdot (1.5 - 0.7)^2} \approx 8$
Technology Based Voltage Scaling

- Exploit velocity saturated sub-micron devices to lower voltage without significant loss in device speed
- Technology based “Optimal” $V_{dd}$: 2.43V for 0.3$\mu$m CMOS

from [Kakumu90]  
*(IEEE Tran. on Electron Devices)*
Supply Voltage Scaling Using $V_T$ Reduction

Threshold voltage reduction enables voltage scaling without performance loss
Optimizing Continuous Mode Circuits

- Optimum $V_{DD}/V_T$ point trades-off switching and leakage power and is a strong function of activity.

also see [Burr94]
Limits of Supply Voltage Scaling

CMOS Inverter Transfer Curves

Output Voltage (V) vs. Input Voltage (V)

$V_{out}$ vs. $V_{in}$

$0.7 \ V = V_s$

$V_{smin} \geq 2-4 \ kT/q$

from [Swanson72]

(IEEE JSSC, April 1972)
Burst Mode or “Event Driven” Computation

<table>
<thead>
<tr>
<th>Trace</th>
<th>Trace</th>
<th>Trace</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Trace Length (sec)</td>
<td>5182.48</td>
<td>26859.9</td>
</tr>
<tr>
<td>$T_{off}$ (sec)</td>
<td>5047.47</td>
<td>26427.4</td>
</tr>
<tr>
<td>$T_{on}$ (sec)</td>
<td>135.01</td>
<td>432.5</td>
</tr>
<tr>
<td>$T_{off}/(T_{off}+T_{on})$</td>
<td>0.9739</td>
<td>0.9839</td>
</tr>
</tbody>
</table>

- For an X-server application, processor spends most of the time in the blocked or off state.

  from [Srivastava95]
  
  *(IEEE Trans. on VLSI Systems)*
Techniques for Burst Mode Computation

Multiple $V_T$ Technology
(Disable high $V_T$ devices during idle periods)

- High $V_T$ transistor sizing issues
- Preserving state requires extra transistors

e.g., [Sakata93] (Symposium on VLSI Circuits), [Mutoh93] (International ASIC Conference)
Latch Design in MTCMOS

From S. Mutoh, et. al.
JSSC, August 1995
Techniques for Burst Mode Computation

Substrate Bias Controlled Variable $V_T$ Devices -
(Increase $V_T$ during idle periods)

from [Seta95] (ISSCC 1995)

- Needs large body factors - large well capacitances
- Triple well process needed
SOI with Active Substrate (SOIAS)

Backgate Control Enables Dynamically Varying Threshold Voltages

from [Yang95]
NMOS Device Characteristics

~ 4 Dec

Vt=0.448 V (Vgb=0.0 V)
Vt=0.184 V (Vgb=3 V)

Leff=0.44 μm
\( t_{si}=4.5 \) nm
\( t_{fox}=9 \) nm
\( t_{box}=100 \) nm
VDS=1.0 V
Ring Oscillator Characteristics

- Processor speed is adjustable on demand
Architectural Model & Activity Parameters for SOIAS

$f_{ga} = \text{Module Activity Factor}$

$b_{ga} = \text{Backgate Switching Activity}$
### Generic Architecture Model for All Technologies

<table>
<thead>
<tr>
<th>Technology</th>
<th>Leakage Control Mechanism (hence affecting $bga$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiple Threshold Technology</td>
<td>Switching the High $V_T$ devices ON/OFF</td>
</tr>
<tr>
<td>Substrate Bias Control</td>
<td>Controlling the Substrate Voltages</td>
</tr>
<tr>
<td>Silicon On Insulator Active Substrate</td>
<td>Switching the Backgate Voltage</td>
</tr>
</tbody>
</table>

**Hierarchy of Profilers and Statistical Models Required for “Virtual Prototyping”**
Energy Estimation Models for SOI and SOI/S

\[ E_{SOI} = \alpha \cdot fga \cdot C_{fg} \cdot V_{dd}^2 \]
\[ + \cdot I_{\text{leak\_lowVT}} \cdot V_{dd} \cdot T_{\text{cycle}} \]

\[ E_{SOIAS} = \alpha \cdot fga \cdot C_{fg} \cdot V_{dd}^2 \]
\[ + \cdot fga \cdot I_{\text{leak\_lowVT}} \cdot V_{dd} \cdot T_{\text{cycle}} \]
\[ + \cdot (1-fga) \cdot I_{\text{leak\_highVT}} \cdot V_{dd} \cdot T_{\text{cycle}} \]
\[ + \cdot bga \cdot C_{bg} \cdot V_{bg}^2 \]

\( fga \) = Module Activity Factor
\( bga \) = Backgate Switching Activity
\( \alpha \) = Node Transition Activity Factor

\( C_{fg} \) is the capacitance associated with the gate.
\( V_{dd} \) is the supply voltage.
\( T_{\text{cycle}} \) is the cycle time.
\( I_{\text{leak\_lowVT}} \) and \( I_{\text{leak\_highVT}} \) are the leakage currents at low and high threshold voltages, respectively.
\( C_{bg} \) is the backgate capacitance.
\( V_{bg} \) is the backgate voltage.
## Architectural Profiling to Determine $fga$ and $bga$

### Table 1. SPEC benchmark espresso

<table>
<thead>
<tr>
<th></th>
<th>Number</th>
<th>$fga$</th>
<th>$bga$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Instructions</td>
<td>900158847</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Additions</td>
<td>543616709</td>
<td>0.6039</td>
<td>0.1954</td>
</tr>
<tr>
<td>Shifts</td>
<td>57000715</td>
<td>0.0633</td>
<td>0.0541</td>
</tr>
<tr>
<td>Multiplications</td>
<td>172883</td>
<td>0.0002</td>
<td>0.0002</td>
</tr>
</tbody>
</table>

### Table 2. SPEC benchmark Li

<table>
<thead>
<tr>
<th></th>
<th>Number</th>
<th>$fga$</th>
<th>$bga$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Instructions</td>
<td>1737729538</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Total Additions</td>
<td>661236960</td>
<td>0.6023</td>
<td>0.2233</td>
</tr>
<tr>
<td>Total Shifts</td>
<td>52224367</td>
<td>0.0087</td>
<td>0.0086</td>
</tr>
<tr>
<td>Multiplications</td>
<td>7088</td>
<td>0.0000</td>
<td>0.0000</td>
</tr>
</tbody>
</table>

### Table 3. Data Encryption (IDEA)

<table>
<thead>
<tr>
<th></th>
<th>Number</th>
<th>$fga$</th>
<th>$bga$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Instructions</td>
<td>2125</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Additions</td>
<td>1250</td>
<td>0.5882</td>
<td>0.2635</td>
</tr>
<tr>
<td>Shifts</td>
<td>186</td>
<td>0.0875</td>
<td>0.0753</td>
</tr>
<tr>
<td>Multiplications</td>
<td>3</td>
<td>0.0014</td>
<td>0.0014</td>
</tr>
</tbody>
</table>
SOI vs. SOIAS Technology Evaluation

Adder

Shifter

Mult.

$\log(\text{ESOIAS/ESOI})$

$\log(\text{front-gate activity factor})$

$\log(\text{back-gate activity factor})$
Transistor Sizing for Low-Power

- Lower Capacitance
  - Small W/L’s
- Higher Capacitance
- Higher Voltage
  - Large W/L’s
- Lower Voltage

- Larger sized devices are useful only when interconnect dominated
- Minimum sized devices are usually optimal for low-power
Transistor Sizing for Fixed Throughput

\[ I \propto \frac{W}{L} C_{\text{MIN}} \]

\[ C_g = \frac{W}{L} C_{\text{MIN}} \]

\[ C_P = C_{\text{wiring}} + C_{\text{DF}} \]

\[ C_{\text{MIN}} = \text{Minimum sized gate (W/L=1)} \]

\[ \frac{W}{L} \text{ after sizing} \]

\[ \alpha = \frac{C_P}{(K C_{\text{MIN}})} \]

HIGH PERFORMANCE

\[ \frac{W}{L} >> \frac{C_P}{(K C_{\text{MIN}})} \]

LOW POWER

\[ \frac{W}{L} = 2 \frac{C_P}{(K C_{\text{MIN}})} \]

(if \( C_P \geq K C_{\text{MIN}} \))

ELSE \( \frac{W}{L} = 1 \)

from [Chandrakasan92]  
(IEEE JSSC, 1992)
# Capacitance Breakdown

## MODULE LEVEL

<table>
<thead>
<tr>
<th>MODULE</th>
<th>GATE</th>
<th>DIFFUSION</th>
<th>INTERCONNECT</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDER (Conventional Static)</td>
<td>30%</td>
<td>45%</td>
<td>25%</td>
</tr>
<tr>
<td>ADDER (Carry Select)</td>
<td>37%</td>
<td>31%</td>
<td>32%</td>
</tr>
<tr>
<td>TSPC COUNTER</td>
<td>32%</td>
<td>26%</td>
<td>36%</td>
</tr>
<tr>
<td>LOG SHIFTER (8 bit shift by 4)</td>
<td>15%</td>
<td>42%</td>
<td>43%</td>
</tr>
<tr>
<td>COMPARATOR</td>
<td>33%</td>
<td>38%</td>
<td>29%</td>
</tr>
</tbody>
</table>

## DATAPATH LEVEL

<table>
<thead>
<tr>
<th>MODULE</th>
<th>GATE</th>
<th>DIFFUSION</th>
<th>INTERCONNECT</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDER CHAIN ( 7 adders )</td>
<td>38%</td>
<td>38%</td>
<td>24%</td>
</tr>
<tr>
<td>WAVE DIGITAL FILTER</td>
<td>31%</td>
<td>29%</td>
<td>40%</td>
</tr>
<tr>
<td>ADDRESS GENERATION (STD CELL)</td>
<td>56%</td>
<td>24%</td>
<td>20%</td>
</tr>
<tr>
<td>VIDEO SYNC GENERATOR (STD CELL)</td>
<td>45%</td>
<td>25%</td>
<td>30%</td>
</tr>
</tbody>
</table>
Choice of Logic Style

CONVENTIONAL CMOS Adder

OPTIMIZED static Adder

DCVSL Adder

CPL Adder
Choice of Logic Style

- Power-delay product improves as voltage decreases.
- The “best” logic style minimizes power-delay for a given delay constraint.
Reducing the Energy/Operation at a Fixed $V_{dd}$

Reduced Signal Swing Example: FIFO Memory

Power Reduction Over Rail-to-Rail Swing $= \frac{V_{dd}}{(V_{dd} - V_t)}$
Reducing the Energy/Operation at a Fixed $V_{dd}$

$E = (RC/t_r)C V^2$ (for $t_r >> RC$)

Applying slow input slopes reduces $E$ below $CV^2$
Useful for driving large capacitors (Buffers)
Power reduction > 4 for pad drivers (1 MHz) $^{ISI}$
Example: Stepwise Adiabatic Driver

From [Svensson94]

\( V_i = \left( \frac{i}{N} \right) V \)

\[
E_{\text{step}} = Q \cdot V_{\text{avg}} = C_L \cdot \frac{V_{dd}}{N} \cdot \frac{V_{dd}}{2N} = \frac{1}{2} C_L \cdot V_{dd}^2 \frac{1}{N^2}
\]

\[
E_{\text{total}} = N \cdot \frac{\frac{1}{2} C_L \cdot V_{dd}^2}{N^2} = \frac{E_{\text{conventional}}}{N}
\]

Activity Driven Logic Level Power Down

from [Alidina94]
(1994 International Workshop on Low-power Design)

- 50% reduction possible for random inputs
Activity Reduction in Shift Registers

N Length Shift Register

\[ P_{\text{serial}} = NC_{\text{reg}} V^2 f_{\text{clk}} \]

N/2 Length Shift Register

\[ P_{\text{parallel}} = 2 \times \left( \frac{N}{2} C_{\text{reg}} V^2 f_{\text{clk}}/2 \right) + P_{\text{overhead}} \]
Shift Register Power for Various Lengths

The graph shows the normalized power dissipation for shift registers of various lengths (32-bit, 64-bit, 128-bit, and 256-bit) as a function of the degree of parallelism. The y-axis represents the normalized power dissipation, and the x-axis represents the degree of parallelism.
Summary

• Power dissipation is a prime design constraint for portable systems
• Low Power design requires optimization at all Levels
• Sources of power dissipation have been analyzed
• Technology, circuit, and logic design techniques have been described
References


