OPTICAL IMEMS® – A FABRICATION PROCESS FOR MEMS OPTICAL SWITCHES WITH INTEGRATED ON-CHIP ELECTRONICS

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ABSTRACT

The ability of silicon micromachining to produce small, precision, movable parts provides an opportunity for MEMS component use in optical communications networks [1,2]. To address this potential market, Analog Devices has developed the Optical iMEMS® process for fabricating MEMS optical components with integrated, on-chip electronics. While this process could be used to make a variety of optics components including mirrors, shutters and actuators for precision alignment, we report here on a MEMS mirror for optical switching. The device consists of a double-gimbaled mirror with on-chip high voltage drive electronics and low-voltage CMOS for capacitive position sense. The mirror can tilt about both the X- and Y-axis, with position sense in both directions of tilt.

BACKGROUND

For a MEMS mirror to be useful in optical communications it must be:

- flat – around >0.1m radius of curvature
- smooth – less than 50Å RMS roughness
- highly reflective – over 90% reflectivity

Although Analog Devices’ Micromachined Products Division is the world leader in surface micromachined polysilicon accelerometers, it was not possible to transfer this technology to the optical switch market place. The polysilicon process could not produce mirrors with the required flatness and smoothness. More importantly, large surface micromachined mirrors have not been able to provide the necessary tilt angles without complicated hinged structures. Such “pop-up” style devices present a number of reliability concerns.

Instead, Analog Devices’ approach to the optical mirror challenge focused on single-crystal silicon as a MEMS structural material. The inherent flatness and smoothness of single-crystal silicon make for an ideal mirror surface. A thin reflective coating can then be applied to achieve the required optical properties. Bulk micromachining a mirror out of a standard silicon wafer is possible, however, the lack of etch-stop layers and electrical isolation between different parts of the substrate limit its usefulness.

Bonded-wafer or SOI-based technologies, bridge the gap between surface and bulk micromachining, combining the best aspects of both methods. A bonded single-crystal silicon layer allows fabrication of millimeter-scale, ultra-flat mirrors with high-strength flexures having micron-scale dimensions. Additionally, the use of a single-crystal silicon MEMS layer provides compatibility with on-chip electronics. The Optical iMEMS® process developed by Analog Devices incorporates all these technological benefits while leveraging ADI’s strength in high volume MEMS manufacture.

FABRICATION PROCESS

The Optical iMEMS® process uses a three-layer silicon stack, as shown in Figure 1. Formed using SOI wafer bonding technology, the triple-stack substrate consists of a 10µm thick mirror layer atop a sacrificial spacer layer (10-80µm thick) fastened to a full thickness handle wafer. Each of the single crystal silicon layers is separated by a bonding oxide that will be used as an etch stop during processing. The handle wafer supports actuation electrodes and interconnects beneath the mirror, and remains solid throughout the process. The solid handle wafer overcomes the issue of through-wafer etching used in other technologies, and provides a robust substrate compatible with ADI’s standard MEMS singulation and assembly techniques.

The sacrificial spacer layer thickness accurately sets the gap between the mirror and the actuation electrodes and can be tailored to meet specific design requirements. In addition to forming the MEMS structure, the 10µm mirror layer can support integrated, high voltage, on-chip electronics.

Figure 1 - Optical iMEMS® Cross Section Schematic

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The Optical iMEMS® wafers start circuit fabrication as trench isolated, bonded wafers with no topology, making them highly compatible with foundry electronics. Clare Inc. provided a 220V DMOS and HVPMOS process with 12V CMOS that forms both the high voltage drive electronics and the lower voltage sense amplifiers. The MEMS portion of the Optical iMEMS® flow adds only 6 masking steps to the circuit process.

**Formation of Buried Polysilicon Electrode Structure**

Tilting mirrors fabricated using the Optical iMEMS® process are actuated electrostatically, and the position of the mirror is sensed capacitively. Both of these characteristics require electrode structures to be formed parallel to the mirror at an accurately controlled distance from the mirror. The actuation and sense electrodes are formed in a layer of doped polysilicon that is separated from the mirror using a fusion bonded sacrificial silicon spacer layer.

A handle wafer is prepared with backside alignment marks, and an LPCVD, phosphorus-doped polysilicon layer is deposited on top of silicon dioxide and silicon nitride dielectric layers. The electrode structure is patterned in the polysilicon by photolithography and etched using DRIE.

LPCVD silicon dioxide is deposited to cap the polysilicon structure before it is bonded to an oxidized silicon wafer. The polysilicon layer can be seen in the Scanning Electron Microscope (SEM) cross-section micrograph in Figure 3(a).

Analog Devices’ Belfast site possesses expertise in high volume, high yield wafer bonding technologies including SOI bonding, silicon-to-silicon direct bonding (Di-BondTM) [3] and over cavity bonding [4]. These core competencies were leveraged to provide a robust manufacturing process for bonding a spacer wafer to the handle wafer. Proprietary CMP processes ensure high strength, void-free bonding.

Wafers are bonded using an EVG850 production SOI bonder and are thinned to the required spacer thickness using grind and CMP processes. Void free spacer layers have been manufactured with thicknesses between 10µm and 80µm +/- 0.5µm.

**MultiBond™ wafer technology**

MultiBond™ is Analog Devices trade name for stacked thick film SOI wafers, and is ideally suited to many MEMS applications [5], including the Optical iMEMS® mirrors. MultiBond™ was used to form the second SOI layer on top of the spacer layer. For the Optical iMEMS® process, this layer is 10µm +/- 1µm of void free single crystal silicon, above a 1µm buried oxide. This silicon layer forms the MEMS structures and also supports the on-chip, integrated electronics.

Figure 2 shows a Spreading Resistance Profile (SRP) through an Optical iMEMS® substrate showing the MultiBond™ SOI and buried polysilicon layers.

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**Deep Via Contacts and Trench Isolation**

In order to contact the electrode layer that is buried under two single crystal silicon layers, Deep Reactive Ion Etch (DRIE) and Reactive Ion Etch (RIE) processes [6] are used to form trenches through the silicon and silicon dioxide layers down to the buried polysilicon layer. The total depth of this etch can be up to 90µm and is enabled by Analog Devices’ DRIE process optimized for etching SOI structures [7].

The etched trenches are lined with a conformal LPCVD coating of silicon dioxide. This oxide is removed from the base of the trench, and the trench is filled with doped polysilicon. The polysilicon forms an Ohmic contact with the electrode layer electrically connecting the wafer surface to the buried sense and actuation pads with a total via resistance of less than 50Ω. The polysilicon is planarized from the surface of the wafer by CMP.

As well as forming via contacts the deep trench structure is used to provide a lateral etch stop for the MEMS release process and for high voltage isolation. The trench thus defines the MEMS region of the device. The structure can be seen in the cross section schematic drawing in Figure 1. Figure 3(a) shows a cross section SEM of a 90µm deep via trench. The trench sidewall isolation and the contact between the polysilicon electrode layer and the polysilicon trench fill can be clearly seen.

A second, circuit isolation trench is also etched and filled through the MultiBond™ silicon layer and the first buried oxide. This trench is lined with LPCVD silicon dioxide and filled with doped polysilicon.

This circuit trench forms dielectrically isolated silicon tubs to enable high voltage device fabrication. Analog Devices has an established technology for trench isolated SOI known as the BCO substrate. In the Optical iMEMS® process, this trench also makes electrical contact with the spacer silicon layer. A SEM image showing a circuit trench is shown in Figure 3(b).
After the trenches are formed, the polysilicon is removed from the surface of the wafer by CMP and the wafer is capped with LPCVD silicon dioxide. The result of this is a wafer that has a planar surface that is compatible with further processing at an integrated circuit foundry.

![Figure 3 - SEM images of (a) via and MEMS isolation and (b) circuit isolation trenches](image)

**HV Circuit Integration**

The on-chip circuit requirements for a MEMS optical mirror chip are two fold:
- 200V transistors for mirror actuation
- 10V CMOS for position sense electronics

Passive elements - resistors, capacitors and interconnect - must also be able to support both voltage ranges. Clare, Inc. of Beverly, MA was selected to provide the integrated electronics for the Optical iMEMS® process. Clare offers a 3µm HVBCDMOS technology built on 10µm SOI that is compatible with the Optical iMEMS® substrate. Key features of the circuit process include:

- Complimentary 220V Lateral HVpMOS and Vertical HVnDMOS technology
- Low Voltage CMOS (+/-12V)
- Medium Voltage (40V) Bipolar NPN/PNP devices
- 3.0µm Minimum Features
- 4.0µm Metal 1 Pitch (2.4/1.6 line/space)
- 8.0µm Metal 2 Pitch (4.6/3.4 line/space)
- Deposited and Plasma Planarized ILD
- Linear Precision 10V Capacitors (1.0F/µm²)
- Folded 400V+ Capacitors (0.1F/µm²)
- Resistors: 20,45,60,200,950,4000,13000 ohms/sq

As the Optical iMEMS® substrate is very similar to standard 10µm SOI material, integration with the Clare circuit process is straightforward. Three integration concerns relate to the pre-existing trench features, namely:
- Aligning circuit layers to existing trench features
- Protecting the trenches through the circuit process
- Contacting the trench vias with Metal 1

The alignment issue is solved with careful matching of stepper field size and alignment targets used by different steppers at Analog Devices and Clare. Protecting the trenches and via posts through circuit process oxidations and etches requires an oxide cap over the features. As this protective oxide cap would hinder the Metal 1 contact to the via posts, an additional mask is added to the circuit process to selectively remove the oxide prior to metal contact. With just these simple exceptions, the Clare circuit process is run exactly as it is on standard substrates.

**MEMS Structure Formation**

Upon completion of the circuit process the MEMS structures are formed in the single crystal silicon device layer. First, the MEMS area must be cleared of all circuit dielectrics. Passivation nitrides and oxides, inter-level metal dielectrics, pre-metal dielectric and gate oxide total over 3µm thick. The bulk of the material is etched away using a dry plasma etch, but the last of the oxide is etched away with a wet HF dip. The final wet etch ensures that the mirror surface remains as smooth as possible, free from any roughening a plasma etch may cause. For MEMS device other than mirrors this would be a secondary concern.

With the silicon surface now exposed, the mirror and suspension pattern are then defined. Photo imaging the tight dimensional tolerances desired on the structure can be a challenge at the bottom of the well formed by the circuit layers. Design rules are required to place critical dimension components, such as the torsional springs, a safe distance from the circuit layer topology. A deep reactive ion silicon etch, of the type used to form the isolation trenches and via posts, etches the 10µm tall MEMS structure stopping on the buried oxide.

**Structure Release**

Releasing the MEMS structure is accomplished in three steps – buried oxide etch, spacer layer silicon etch, and wet HF oxide etch. All three of these etches are accomplished with a single photoresist masking step. Not only must the resist stand up to all three etches, it must be strong enough to support the mirror and prevent the structures from moving at anytime during the release process. The patterns formed in this masking step are 8µm wide etch holes that must be cleared to the bottom of the 10µm tall mirror structure. This highly challenging photolithography step was implemented using a two layer resist coating, convection oven baking and focus drilling to expose the entire resist thickness.

The first etch is a dry plasma etch through the 1µm bonding oxide between the device and spacer layer. These holes etched in the buried oxide allow access to the silicon spacer layer which is etched using an Xactix XeF₂ etch system. The XeF₂ etch show selectivity of over 1000:1 between the silicon and both the photoresist and oxide, allowing a long etch and extreme undercut between etch holes spaced up to 200µm apart [8]. The XeF₂ is confined to the cavity below the mirror by the bonding oxides on the
top and bottom of the spacer layer and laterally by the oxide lining on the trench surrounding the MEMS region.

After XeF$_2$ etching, a wet HF etch is used to remove all the oxide etch-stop layers in the cavity below the mirror. Removing the oxide on the back of the mirror is especially important, as the 1µm thick film would introduce substantial mirror curvature if left behind. Lastly, a gentle oxygen resist ashing provides a dry, stiction-free release of the MEMS structure, as is done in ADI’s production accelerometer process.

To improve mirror reflectivity, a thin layer of gold and associated adhesion and barrier metals is evaporated onto the released mirrors using an aligned shadow mask. Although the reflective metal stack is only present on one side of the mirror, the 10µm thick silicon mirror is stiff enough to limit curvature induced by evaporated layers. After the final packaging process bakes, the mirror has a radius of curvature greater than 0.1m.

Completed Mirror Chip

Figure 4 - SEM photo of Optical iMEMS® Mirror with integrated circuits

Figure 5 - SEM photo showing via post interconnect to mirror sense and actuation pads

Figure 6 - Simplified schematic of the mirror and position-sense signal path (configured for x-axis sensing)

A source of error is introduced into the sense path by motion of the mirror during the sensing period. Since the capacitance between actuation electrodes and the mirror change with motion, large static actuation voltages cause an error current roughly proportional to mirror velocity. This velocity feed-through error can be destabilizing because, for certain motions, it acts as negative damping in feedback. Chopper-stabilization of sense pulse polarity, at 10kHz, is used to attenuate the effect of velocity feed-through, as shown in Figure 6 [9]. Since velocity feed-
through is independent of sense-pulse polarity, velocity feed-through remains about DC, while the desired mirror position signal is translated to 10kHz. After an ADC and a digital high-pass filter (which reduces energy near DC), the position is digitally demodulated. Residual feed-through errors, as well as offset, are translated to 10kHz, above the mirror servo-loop bandwidth. This sense-pulse modulation provides additional advantages, including substantial improvements in long-term drift and offset with a minimal amount of additional phase error.

EXPERIMENTAL RESULTS

Experimental results were gathered from both a fully integrated mirror test chip, and a circuit-only test chip with metal-poly dummy capacitors to emulate mirror capacitance. Figure 7 shows measured capacitive position sense output voltage for Y-axis mirror rotation versus feedback electrode voltage. Feedback voltages are applied under four different electrode configurations. Note the good rejection of the sense interface to X-axis rotations, applied by the combinations of electrodes 2 and 3. The full-scale input capacitance change of the dummy mirror chip circuit was +/- 8fF with a signal-to-noise ratio of 84dB in a 2kHz bandwidth. Sense pulse modulation proves highly effective in rejection of sources of error arising in the sense circuitry, including offset and supply coupling.

![Figure 7. Plot of Y-Axis output vs. force-electrode voltages. Different sweeps represent application of voltages to different electrode combinations](image)

Table 1 - Design Parameter Comparison of ADI 2μm polysilicon process and Optical iMEMS® Process

<table>
<thead>
<tr>
<th>Design Parameter</th>
<th>2μm Polysilicon</th>
<th>Optical iMEMS®</th>
<th>Gain</th>
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</thead>
<tbody>
<tr>
<td>Structure Thickness</td>
<td>2μm</td>
<td>10μm</td>
<td>5x</td>
</tr>
<tr>
<td>Structure Curvature</td>
<td>0.2μm</td>
<td>10μm</td>
<td>50x</td>
</tr>
<tr>
<td>Structure Roughness</td>
<td>50Å RMS</td>
<td>5Å RMS</td>
<td>10x</td>
</tr>
<tr>
<td>Spacer Thickness</td>
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<td>80μm</td>
<td>40x</td>
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<tr>
<td>Actuation voltage</td>
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<td>200V DMOS</td>
<td>8x</td>
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Now that a single mirror has been demonstrated, the technology can be scaled to mirror arrays for multiple fiber switching applications.

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REFERENCES