Experiments and Models for Circuit-Level Assessment of the Reliability of Cu Metallization

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Abstract

Accurate circuit-level reliability analyses can be based on experimental results for simple interconnect segments if interconnect trees, linked interconnect segments within one level of metallization, are used as fundamental reliability units. The reliability behavior of both segments and trees is different for Al and Cu. A revised method is proposed for tree-based circuit-level reliability analyses for Cu. The types of additional experimental data that would allow assessments with improved accuracy are outlined.

Introduction

The ITRS projects that exponentially increasing number of interconnect segments will be required to carry increasing current densities in the years to come. Both trends separately require rapid improvements in interconnect reliability. This requirement must be met during a period in which metallization technology is evolving at an unprecedented rate. As a consequence, rapid evolution of the methods used to assess the impact of technology changes on IC reliability is also required.

Circuit-Level Reliability Assessments

Circuit-level assessments carried out at the design and layout stages allow more accurate reliability projections, and also allow technology and layout changes that will lead to improved reliability with still-optimized performance. In developing circuit-level reliability analyses, it must first be recognized that the number of different interconnect configurations seen in circuits greatly exceeds the number of configurations that are characterized in experiments. Traditionally, electromigration test structures consist of interconnect segments that terminate at vias that connect to other layers of metallization (Fig. 1a). These structures are often characterized individually as well as in chains. Most interconnect segments in circuits connect with one or more segments in the same layer of metallization. The key to accurate circuit-level reliability assessments is determining how to use data obtained from individual unlinked segments to assess the reliability of the vast array of linked-segment configurations found in circuits.

At least 3 approaches to this problem have been pursued. The most traditional approach is to treat all segments of a given width as if they were linked in series, and apply a line-length-dependent reliability model. However, given that in modern Al technology, and probably also in Cu technology, most electromigration failures are associated with atomic flux divergences at vias, this approach does not accurately address either the positive (1) or negative effects that vias can have on interconnect reliability. An alternative approach is to treat the reliability of segments independently, regardless of their linkages and the stress conditions of linked segments. However, it has now been shown for both Al-based (2) and Cu-based (3) metallization that the reliability of a segment depends very strongly on what it is linked to. This dependence can be both positive and negative, so that segment-level reliability analyses are neither consistently conservative nor optimistic, but are consistently inaccurate.

The third approach is to base circuit-level analyses on assessments of the reliability of interconnect trees (4). An interconnect tree is defined as a collection of segments that are linked within a layer of metallization (Fig. 1b). As long as the vias between layers of metallization block electromigration, the reliability of interconnect trees can be treated independently in circuit-level analyses. In Al-technology, the condition that vias be blocking is satisfied by the presence of W, and in Cu technology, the condition is generally satisfied by the presence of refractory metal liners at the base of vias. Electromigration-blocking boundaries at vias can affect the length dependence of tree reliability in a positive way.

Length Effects

The evolution of hydrostatic stress \( \sigma \) as a function of time \( t \) and length along the interconnect \( x \) can be described by

\[
\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x} \left[ DB \left( z^* q \rho \gamma - \Omega \frac{\partial \sigma}{\partial x} \right) \right]
\]  

[1]
where D is the effective diffusivity, B is an effective elastic modulus that characterizes the elastic response of the material that surrounds the electromigrating material, \( z^* \) is the effective charge, q is the fundamental electronic charge, \( \rho \) is the resistivity, j is the current density, \( \Omega \) is the atomic volume, k is the Boltzmann’s constant, T is the temperature, and the left and right hand terms in the parentheses account for the flux due to the electron wind force and the back-flux due to stress gradients, respectively (5).

Generally, the product of \( z^* \) and D is determined through experiments, and both \( z^* \) and D are affected by which one of a number of diffusion mechanisms dominates. In Al, if grain boundaries are aligned along the direction of electron and atom flux, diffusion along grain boundaries dominates. In Al with bamboo grain structures and in undoped Cu, diffusion along interfaces dominates.

In a simple via-terminated segment such as the one shown in Fig. 1a, electromigration leads to accumulation of atoms and a tensile stress at the cathode end, and depletion of atoms and a tensile stress at the cathode end (Fig. 2). If the stress required for nucleation of a void (\( \sigma_{nuc} \)) is exceeded at the cathode, a void will form and grow, possibly leading to an open-circuit or resistance failure. If the stress required to cause an extrusion is reached (\( \sigma_{ext} \)), generally through dielectric cracking or liner failure, an extrusion will form, possibly leading to a short-circuit failure. However, if a line has a sufficiently short length \( L \) or is stressed at a sufficiently low j, a steady state stress distribution will develop for which neither \( \sigma_{nuc} \) or \( \sigma_{ext} \) is reached, and electromigration will not lead to failure (Fig. 2a). In this case the line is often referred to as “immortal”. This condition is reached when the electron wind force is balanced by the back-stress. This condition was first described by Blech (6) for a similar effect in different structures, for which it was shown that the product of j and L below which a segment would be immortal is given by

\[
jL < (jL)_{nuc} = \frac{\Omega |\Delta\sigma_{ext}|}{z^* q \rho}
\]

where \( \Delta\sigma_{ext} = \sigma_{nuc} - \sigma_{ext} \).

Al interconnects often have overlayer refractory metal anti-reflection coatings as well as refractory metal underlayers (e.g., TiN). These layers do not electromigrate under relevant conditions, so that once voids form in Al interconnects, current can shunt around the voids. In this case, current will continue to flow and the resistance of the segment will increase as the void grows. In short lines or lines stressed at low current densities, void growth will stop when a steady state is reached (Fig. 2b). The resistance will then grow to a finite value and “saturate”. If the saturation resistance is at or below the defined failure resistance, the line will again be immortal (1). This will happen when

\[
jL < (jL)_{sat} = \frac{(\rho / A) \Delta R_{fail}}{2 \Omega B R} \frac{2 \Omega B}{q z^*}
\]

where \( \Delta R_{fail} \) is the defined resistance increase for failure, and \((\rho / A)\) and \((\rho / A)_l\) are the ratio of the resistivity to the cross-sectional area of the Al and liner, respectively (7). This is a less stringent condition than that given in Eq. [2]. For modern Al technology, \((jL)_{sat}\) is about 4000 A/cm (8).

Riege and co-workers showed that for an interconnect tree, an effective jL product could be defined for use in determining whether trees are immortal according either the criteria given in Eq. 2 or 3 (4, 9). To find the effective jL product for a tree, the sums of the jL products for the segments, i, in all possible paths through the tree must be determined. The effective jL product is then given by the largest sum,

\[
(jL)_{eff} \equiv \sum_{i} j_i L_i
\]

This result is the basis for hierarchical tree-based reliability analyses (4).

**Cu vs. Al**

In current Cu technology, the refractory metal liner on the sides and bottom of lines can shunt current around a void, but the non-conducting diffusion-barrier/etch stop on top of the Cu (e.g. SiN) can not. This leads to fundamentally different behavior in simple via-terminated segments in undoped-Cu compared to Al. First, it has been shown for a range of line lengths and widths that the median times to failure \( t_{50} \) in lines terminating with vias below the test line (Fig 3b), are significantly higher than for segments terminating at vias above the test line (Fig. 3a) (10). This is due to the ease with which voids nucleate at the Cu/etch-stop interface. In via-below structures, voids that nucleate...
at this interface must grow to relatively large sizes to cause failures, whereas in via-above structures, relatively small voids can cause failure (Fig. 3).

In separate studies, it has also been found that via-below segments and via-above segments of undoped Cu have different critical J_L products, 3700A/cm (11) and 1500A/cm (12), respectively. These differing results are also associated with the differences in void locations. The experimental J_L product for via-below structures corresponds to (J_L)_sat, while the J_L product for via-above structures is close to (J_L)_nuc.

Another important difference between Cu and Al interconnects was demonstrated by Hu et al (13), who tested segments terminating at one end with a via above the line and terminating with a via below the line at the other end. The most important characteristic of these segments was that the via-above had a very thin liner while the via below had a relatively thick liner. As a consequence, the lifetime of these segments depended strongly on the direction of current flow. This was interpreted to be the result of rupture of the thin liner. When the thin liner was the anode, liner rupture led to rapid voiding at the strong liner. When the thick liner was the anode, rupture of the thin liner allowed the cathode lead to act as a reservoir for Cu, and voiding was delayed.

A Tree-Based Reliability Assessment Methodology for Cu Metallization

In view of the differences outlined above, the hierarchical tree-based reliability assessment methodology developed for Al (9) must be modified for Cu as shown in Table I. If it can be assumed that all vias have electromigration-blocking liners, the substantive modification is to separately treat segments with via-above and via-below configurations, defaulting to the conservative via-above criteria when trees have a mix of both types of vias. If liners at vias might not be blocking, analyses become more complex. Non-blocking boundaries could be assigned according to various algorithms, including randomly. If non-blocking vias link immortal metallization in two or more layers of metallization, a larger mortal tree could be created, thereby increasing the number of mortal trees. Non-blocking boundaries can also link two or more mortal trees to form a single larger mortal tree, thereby reducing the number of mortal trees. Whether the latter effect leads to a reliability improvement depends on how strong the size dependence of mortal trees is. If the size dependence is weak, non-blocking boundaries could, in principle, lead to a reliability improvement. In the more likely event that the size dependence is relatively strong, non-blocking boundaries will lead to a reliability degradation.

A new tool, called SysRel, has been developed for circuit-level reliability assessments of either Al-based or Cu-based metallization (14). This tool extracts trees from circuits laid out using Magic (15) or 3DMagic (16) and applies the tree-based methodology outlined in Table I, with changes for Cu in bold. This tool has so far been used to analyze relatively small circuits. These analyses indicate that Al-based (bamboo) and undoped-Cu-based metallization have similar reliabilities. It has also been found that random introduction of a sub-population of non-blocking boundaries leads to a reduction in the number of mortal trees. Analyses of larger circuits are needed to determine if these results are general. Also, the impact of non-blocking boundaries requires better experimental characterization using test structures designed to probe the likelihood and conditions for liner rupture, and designed to probe the size dependence of the reliability of mortal trees.

Summary

A modification of the hierarchical tree-based reliability analysis developed for Al has been developed for Cu. Using a new tool based on this method, it has been found that bamboo Al and undoped Cu have similar reliabilities. Perhaps the most important difference between Cu and Al technology is the possibility that the liners in vias might not block electromigration. New experimental results based on new test structures are needed to accurately assess the impact of non-blocking vias on the reliability of Cu-based metallization.

Table I

<table>
<thead>
<tr>
<th>Hierarchical Circuit-Level Reliability Analysis for Cu</th>
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</thead>
<tbody>
<tr>
<td>1) Extract trees from layout.</td>
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<tr>
<td>2) Apply blocking boundary rule:</td>
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<tr>
<td>- all vias block,</td>
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<tr>
<td>- vias at ends of long segments do not block,</td>
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<tr>
<td>- randomly distributed non-blocking vias.</td>
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<tr>
<td>3) Link trees connected with non-blocking vias.</td>
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<td>4) Segregate via-up and via-down trees (worst case: via-</td>
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<tr>
<td>up)</td>
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<tr>
<td>5) Apply (J_L)_nuc or (J_L)_sat filters for worst-case</td>
</tr>
<tr>
<td>j's.</td>
</tr>
<tr>
<td>6) Make current estimates for remaining trees.</td>
</tr>
<tr>
<td>7) Apply (J_L)_nuc or (J_L)_sat filters for estimate</td>
</tr>
<tr>
<td>currents.</td>
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<tr>
<td>8) Apply tree-size-dependent default model.</td>
</tr>
</tbody>
</table>

References